CBC2: front-end readout ASIC for the High-Luminosity Upgrade of the CMS Strip Tracker

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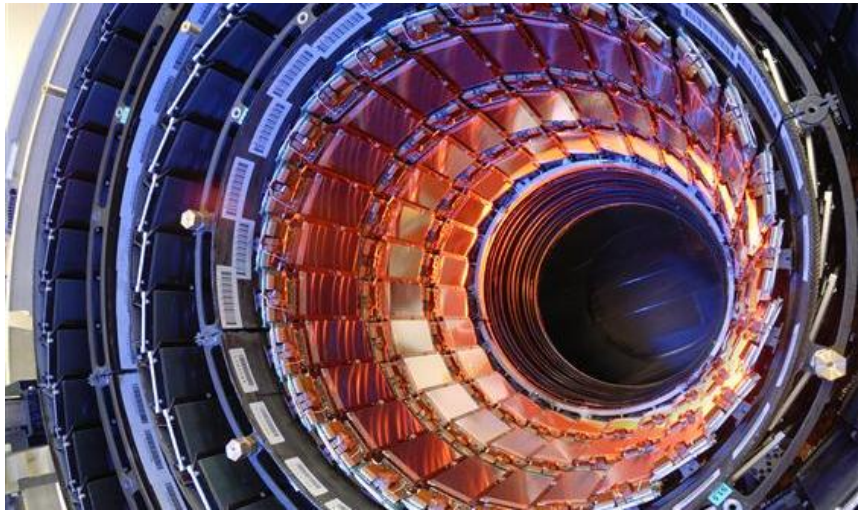
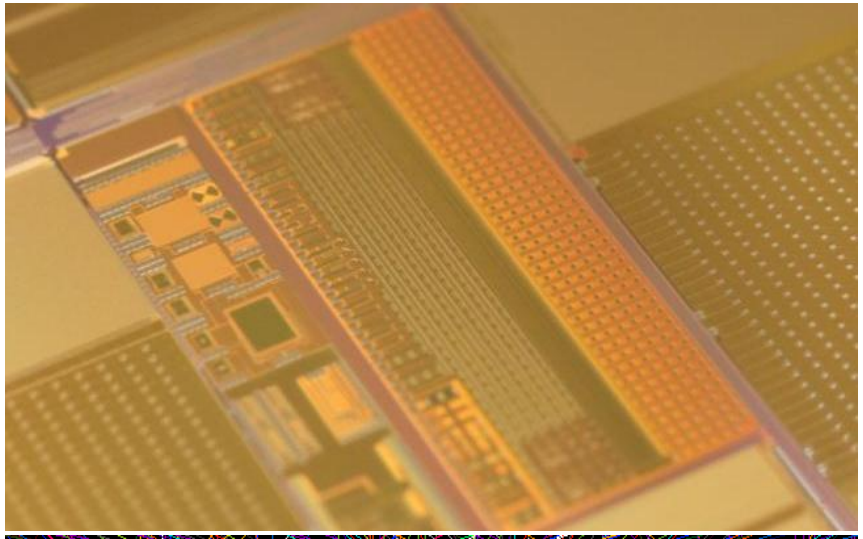
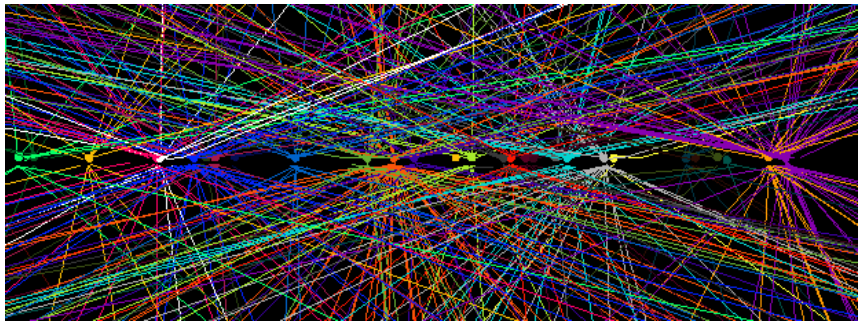


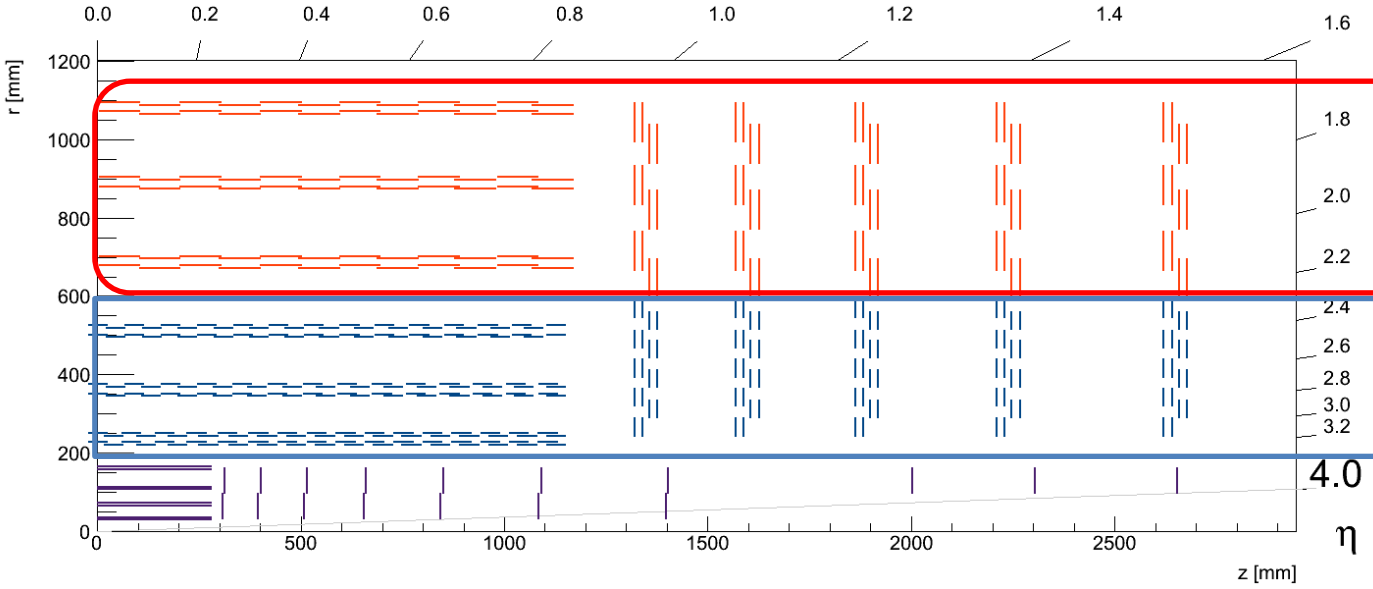




Outline

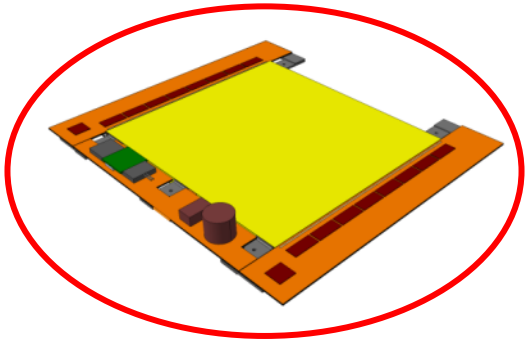
- Tracker upgrade & detector module
- The CMS Binary Chip 2 (CBC2)
- CBC2 architecture
- CBC2 performance
- CBC2 testing
  - Beam test
  - TID test
- Summary & Conclusion

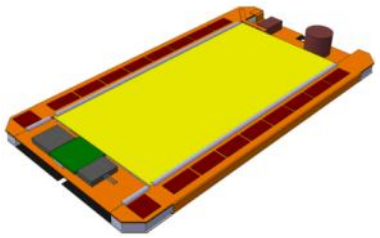
Phase-II upgrade of the CMS Strip Tracker



2S strip-strip double-layers
~8400 modules
~34M channels
~155m^2

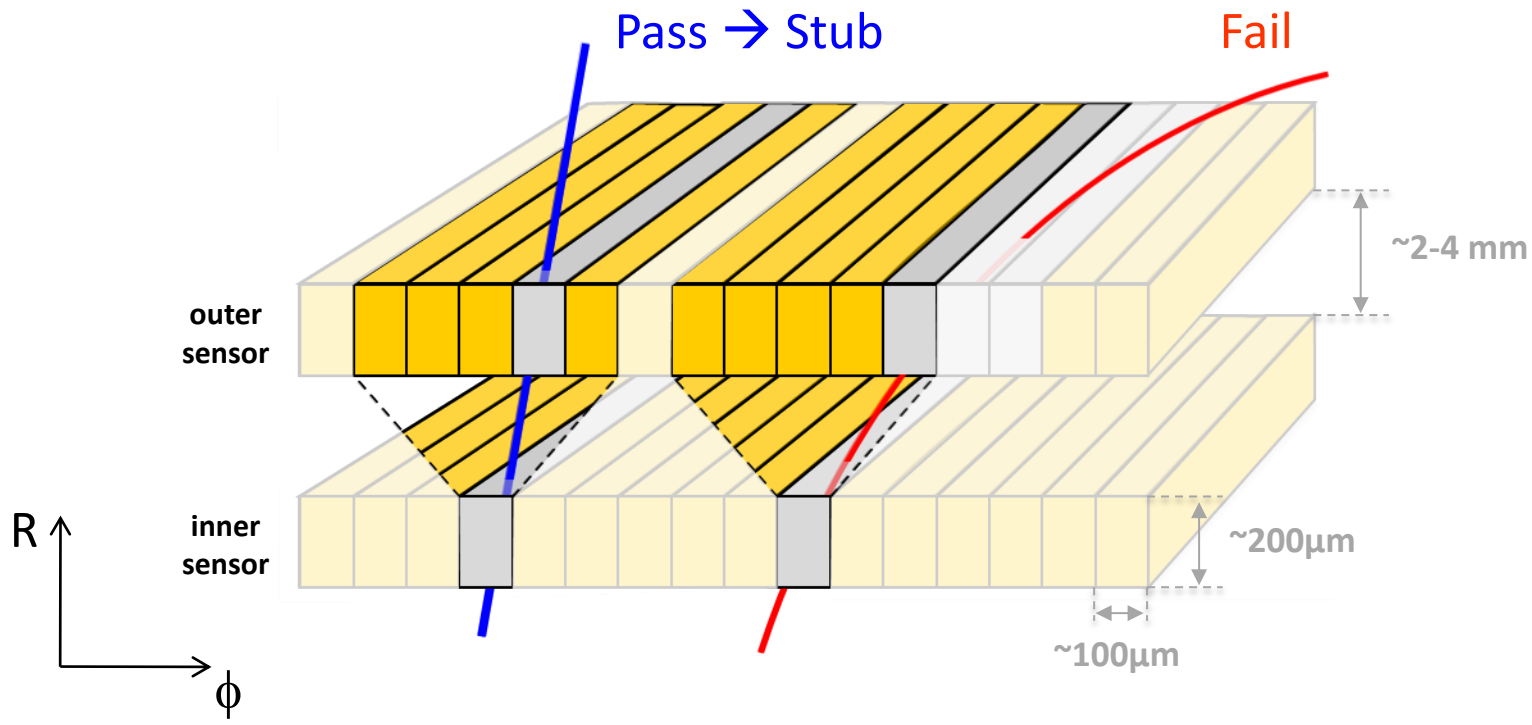
PS strip-strixel double-layers
~7000 modules
~230M channels
~62m^2





- Baseline design: Barrel+5Endcaps
- Based on 2 module types only
- Provides at the same time:
  - *readout data* upon receipt of L1 trigger
  - *trigger data* @40MHz

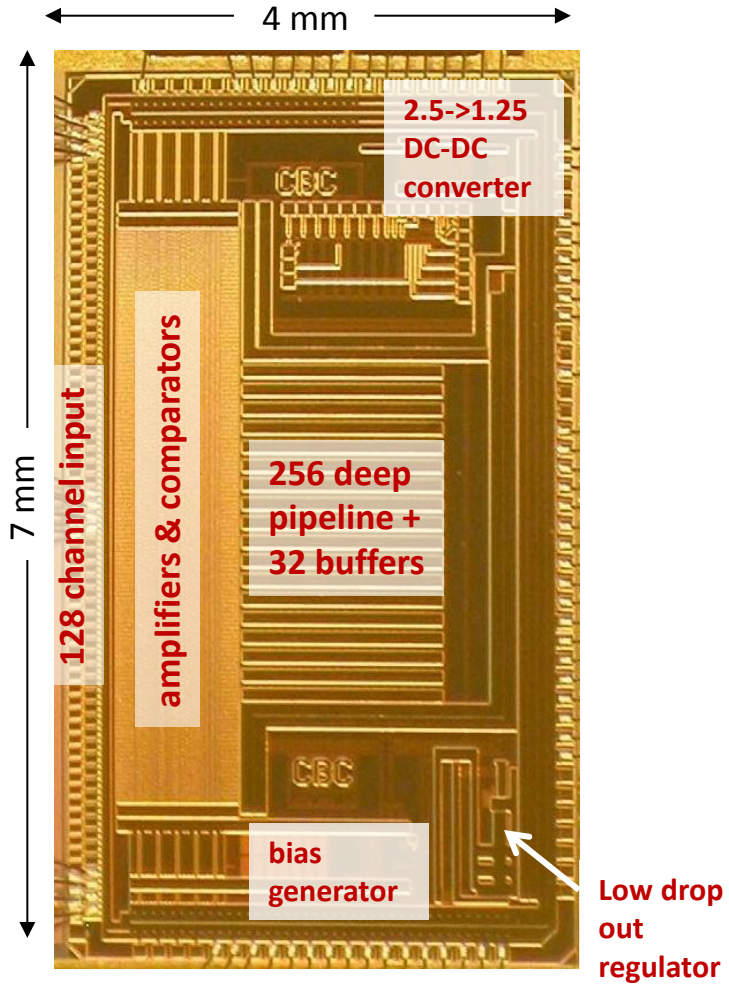
Basic trigger module concept

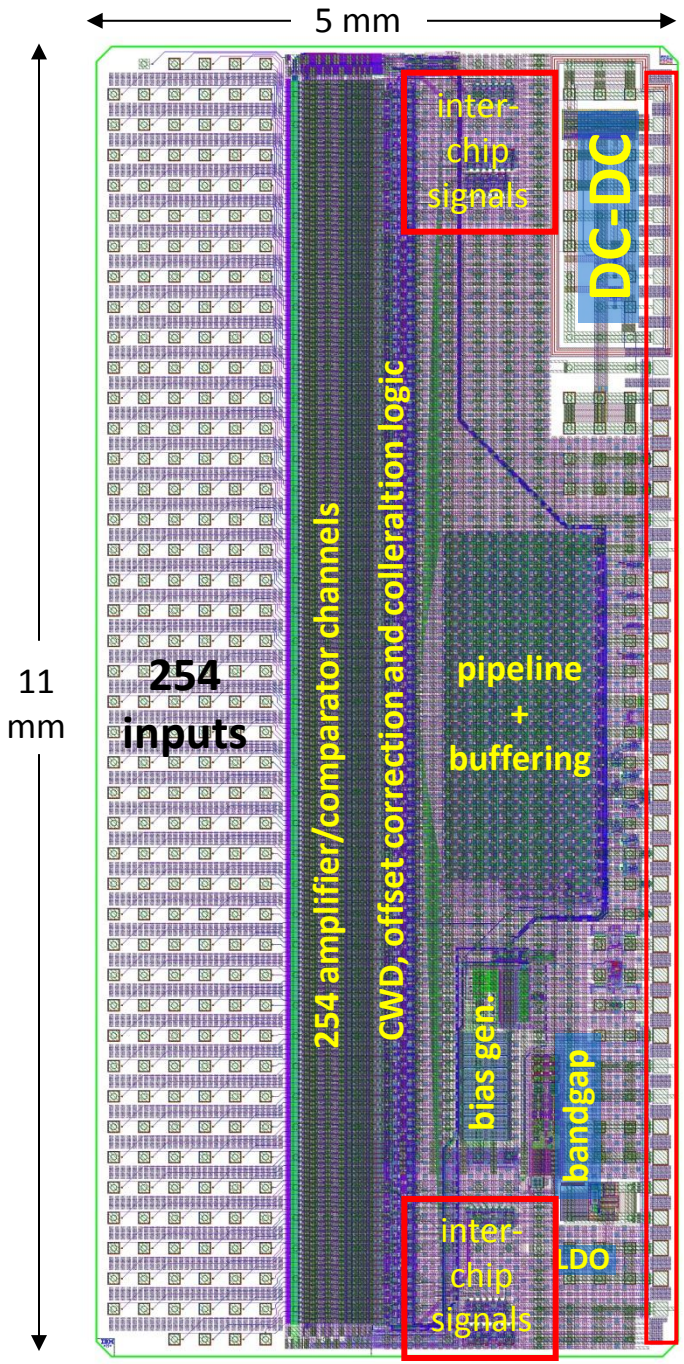


- High-PT tracks (stubs) can be identified if cluster centre in top layer lies within a search window in R-Φ (rows)
- p_T cut given by: module radius (z), sensor separation and correlation window

First version: CBC main features

- IBM 130nm CMOS process
- binary, unsparsified architecture
  - retains chip and system simplicity
  - but no pulse height data
- designed for ~2.5 - 5cm µstrips < ~ 10 pF
- 128 channels, 50 µm pitch wire-bond
  - either polarity input signal
- **not contributing** to L1 trigger
- powering test features:
  - 2.5 -> 1.2 DC-DC converter
  - LDO regulator (1.2 -> 1.1) feeds analogue FE
- fast (SLVS) and slow (I2C) control interfaces





CBC → CBC2: New Features

- 250µm pitch C4 layout
  for commercially assembled module
  back edge wire-bond pads for wafer probe
- 254 channels for 127 + 127 strips
- correlation logic for stub formation
  between top & bottom strips
  vetoes wide clusters
- Front-end circuit improvements
- On-chip test pulse circuit
- Improved DC-DC (CERN)
- received Jan 2013 – fully functional

CBC2 overview

254 Channels
- Preamp
- Postamp
- Comparator

Stub-finding logic
- Cluster width discriminator
- Offset correction
- Coincidence logic
- Inter-chip signals

Pipeline memory 256 deep
- Dual-port RAM, no SEU immunity

Buffer Memory 32 deep
- Pipeline address has Hamming encoding

Programmable Biases

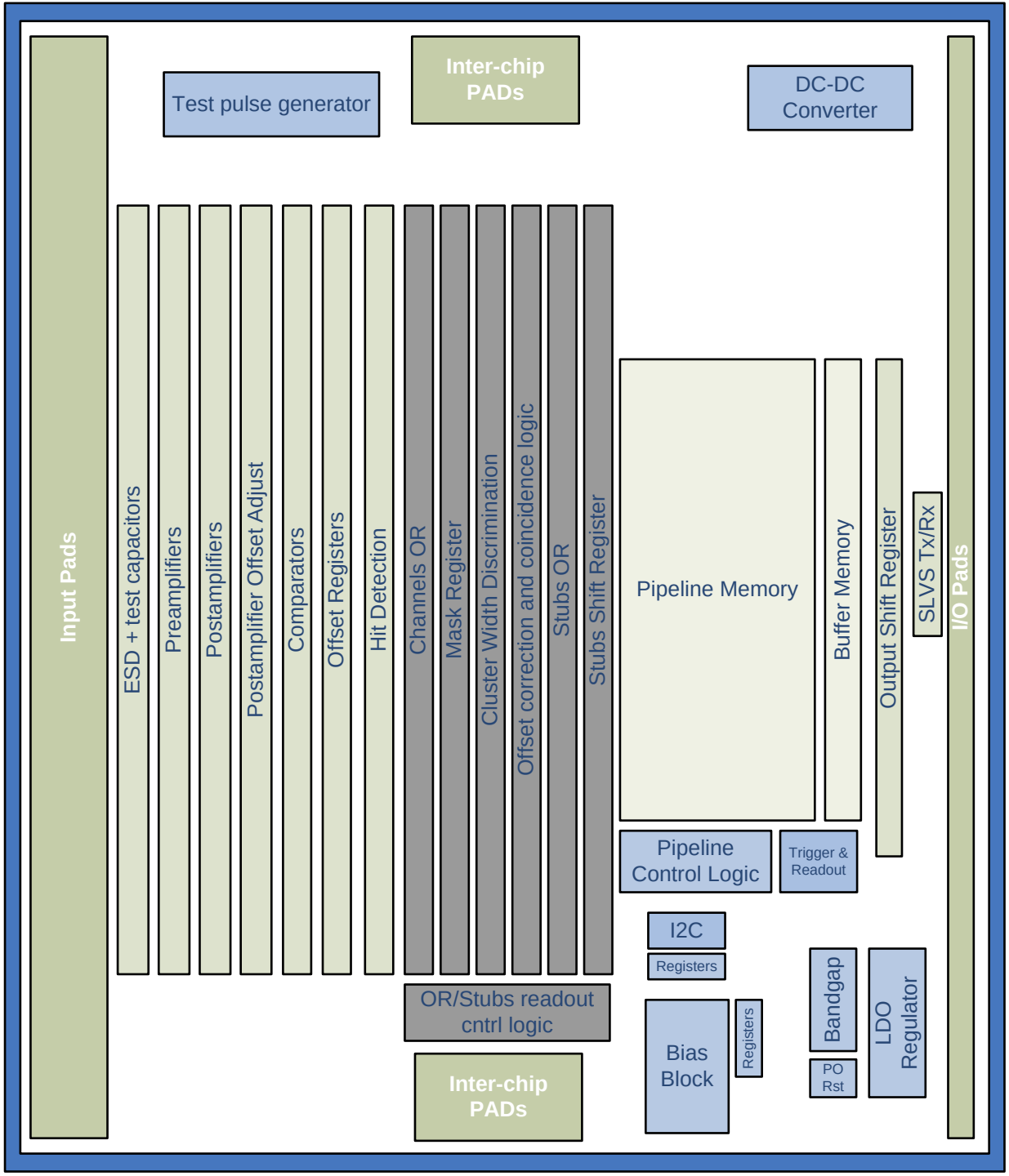
Bandgap

LDO Regulator

DC-DC Converter

I²C Interface

SLVS I/O

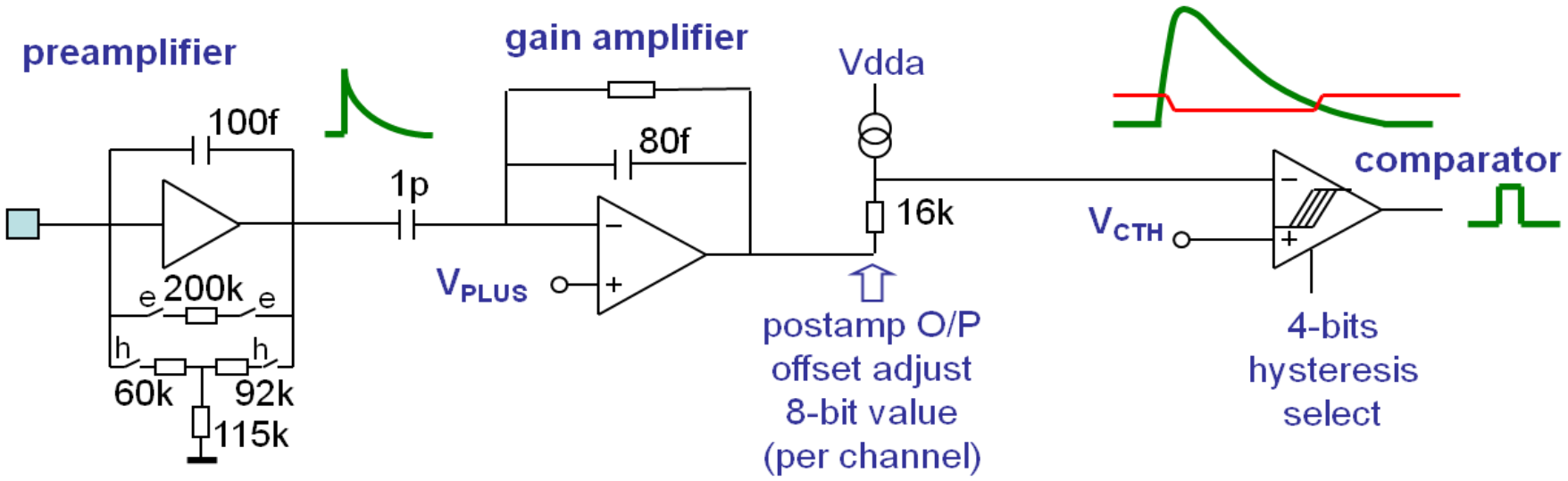


Front End: Design

CBC2 Front End Specifications

Detector Type:	Silicon Strip
Signal Polarity:	both (electrons and holes)
Strip length:	2.5 – 5cm
Strip Capacitance:	< 10pF
Coupling:	AC or DC
Detector leakage:	up to 1uA leakage current compensation
Noise:	<1000e^-_{RMS} for 5pF sensor capacitance
Overload recovery:	normal response within ~ 2.5µs after 4pC signal
Power:	~500µW / channel (for 5pF strips)
Power supply:	1.1 V (front end supplied through LDO to get supply noise rejection)
Gain	50mV/fC
Dynamic range:	Linear up to 4fC
Timewalk:	<16ns for 1.25fC and 10fC signals with comp. thresh. set at 1fC

Front end



PreAmplifier:

- 100fF feedback capacitor
- Selectable resistive feedback network for leakage current of both polarities
- 20ns time constant

Gain Amplifier:

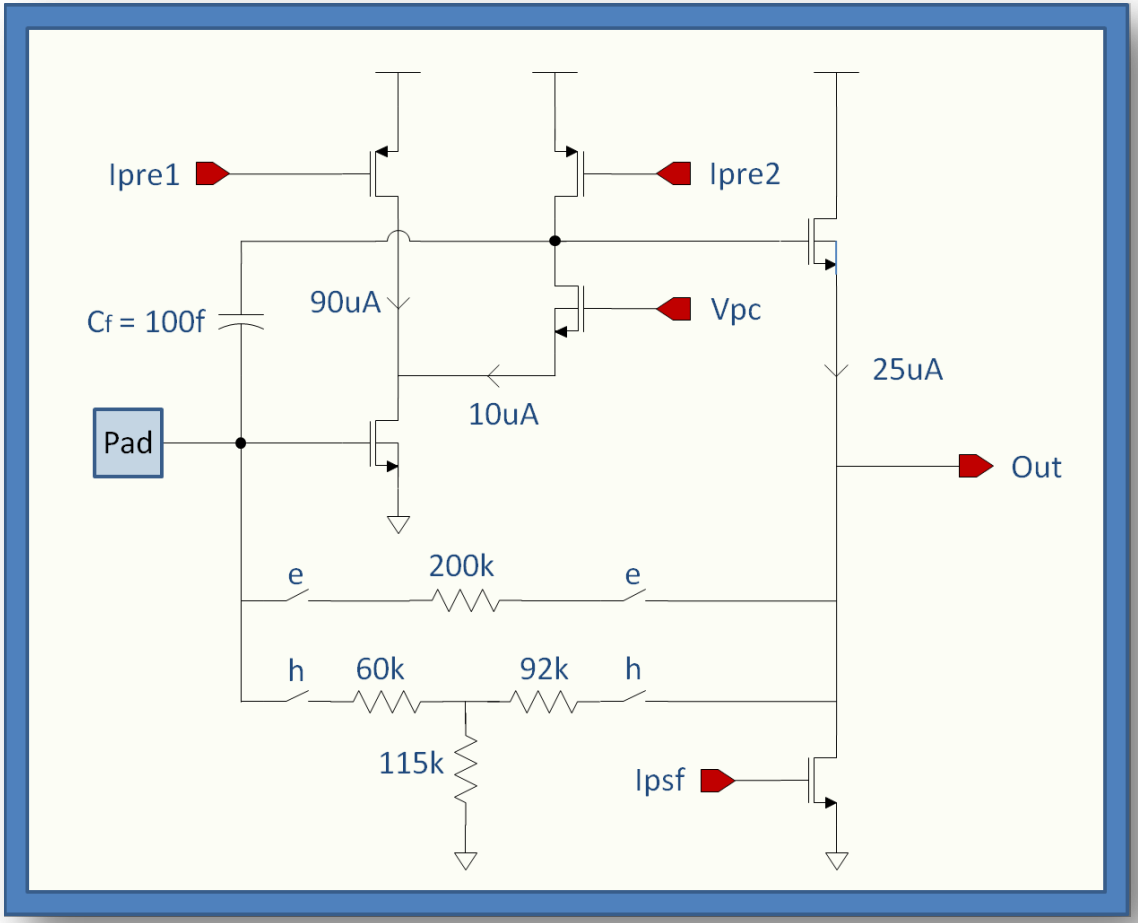
- Designed for both e^- and h^+
- Coupling capacitor removes leakage current shift
- Offset programmable independently for every channel (8b)

Comparator:

- Global threshold (8b)
- Internal programmable hysteresis

Charge Sensitive Preamplifier

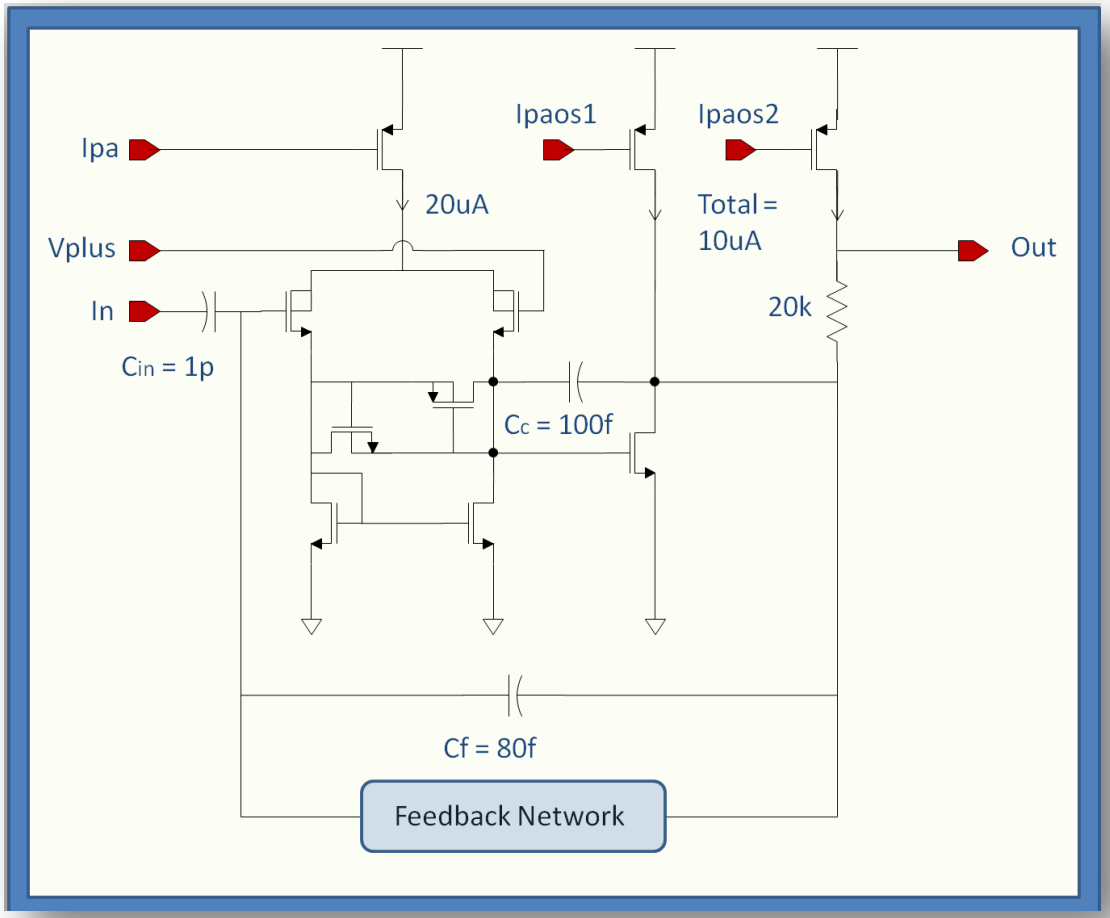
- Single ended cascode + source follower
  - nMOS input to reduce power supply noise
  - 1/f corner quite low

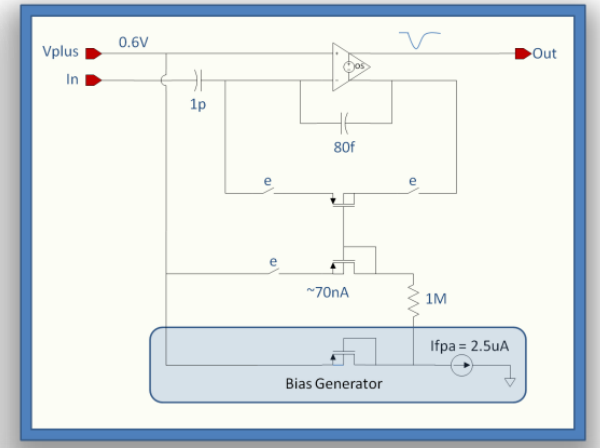


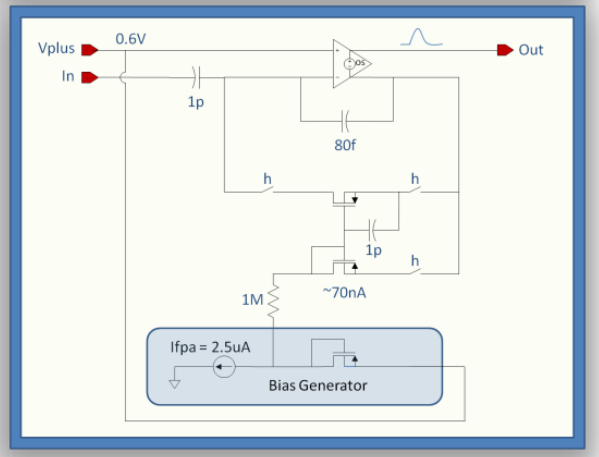
- Cascode and input devices optimized independently
- Selectable resistive feedback for e^- and h^+
  - T-network in holes mode to increase headroom with leakage shift
- 20ns peaking time

Gain Amplifier

- 2stage differential, inverting
- AC-coupled to preamp
- x 12.5 gain
- Diode-connected transistors improve recovery time for very large (HIP) signals
- Selectable e^- and h^+ feedback network
- 8b selectable currents

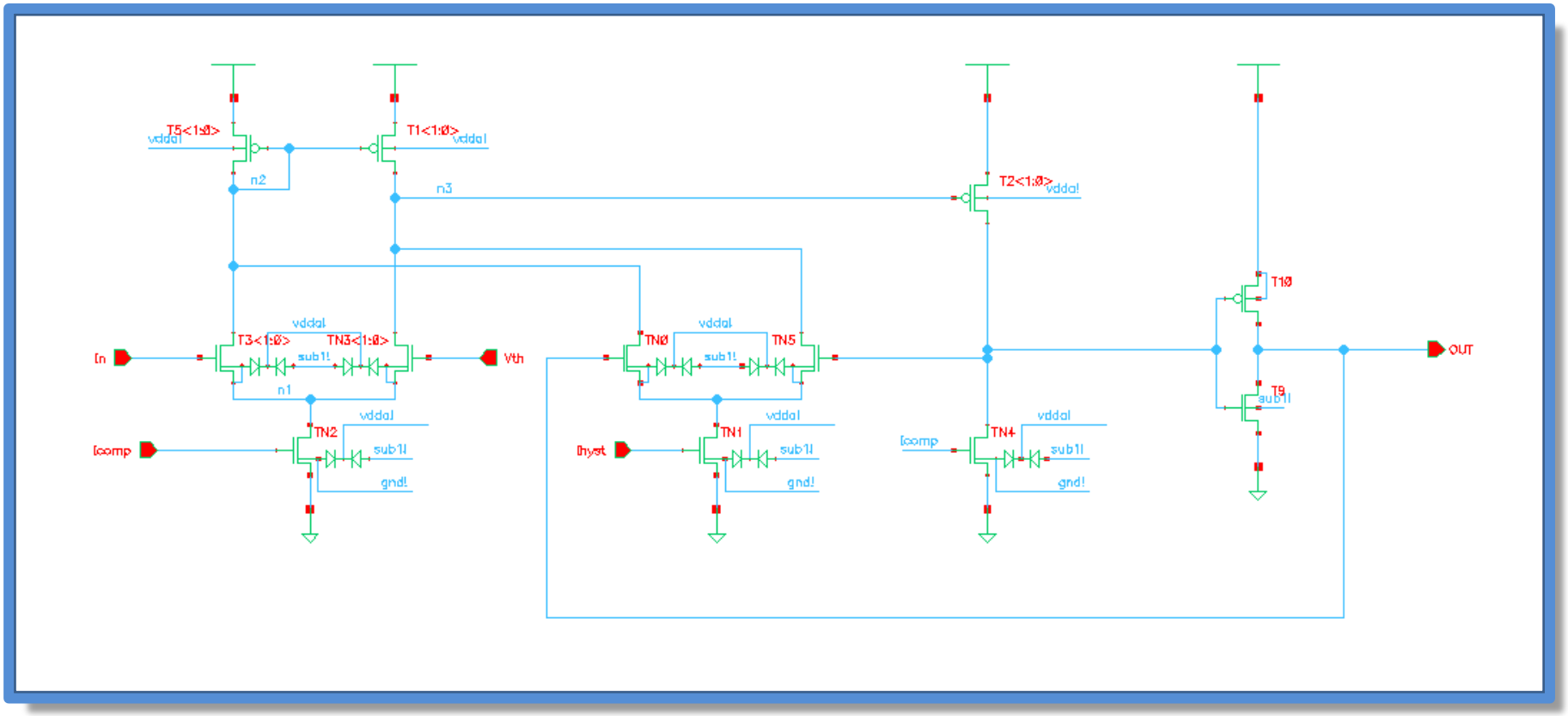




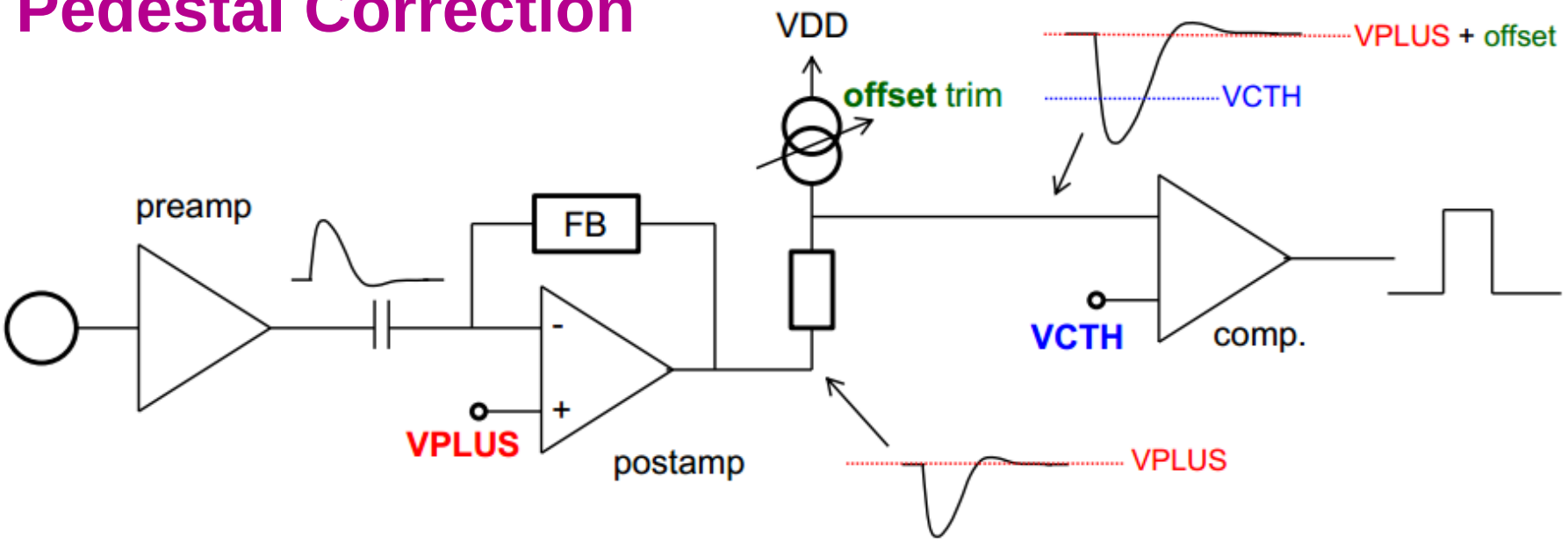


Comparator

- 2-stage differential
- Internal programmable hysteresis (4b global)
- Transition from analog/digital domains
- Timewalk within specs
- Comparator and gain amplifier pedestals corrected in one step with programmable DC-shift of comparator input
- 2 modes of operation: normal return to baseline or 25ns-pulsed



Pedestal Correction



3 voltage levels to program:

VPLUS sets DC point at output of postamp
Offset current adds an extra positive DC shift
VCTH is the comparator threshold

VPLUS, **VCTH** are global (same value for all channels)
Offset current is individually adjustable for every channel

Tuning procedure:

1. Set all **offsets** to a value not too small (to avoid slew-rate limiting at comparator input node
2. Set **VCTH** in middle region of input range
3. Sweep **VPLUS** to find value corresponding to average channel s-curve midpoint (1/2 channels firing) → This is the final value for **VPLUS**
4. Tune channel offsets to achieve midpoint on **VCTH** → tune pedestal (not using test pulse) for few channels at once

Front End: Test Results

Gain measurements

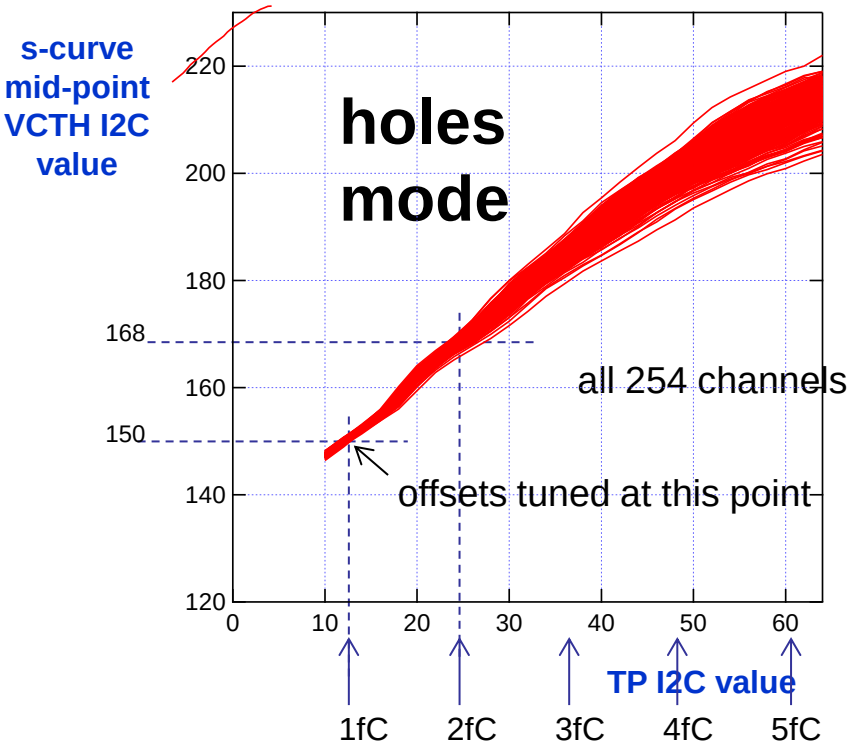
sweep global comparator threshold VCTH
to get s-curves for range of test pulse amplitudes

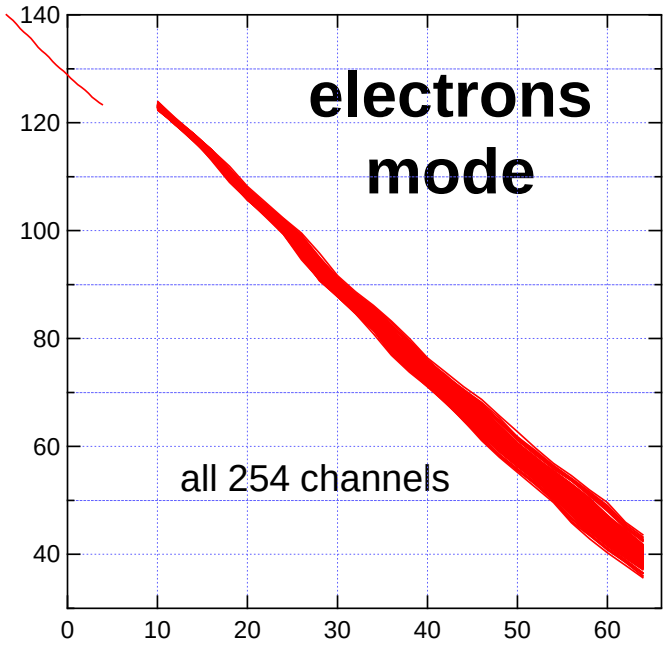
plot s-curve mid-points vs. TP amp

rough calculation in 1÷2fC region
(assumes TP value of 12 / fC)

(168 - 150) x 2.5 mV* = 45 mV/fC

(* from VCTH bias sweep measurements)



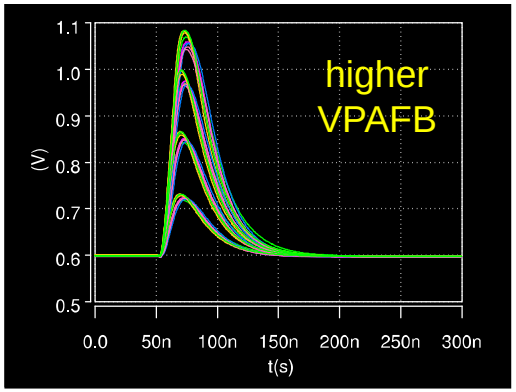


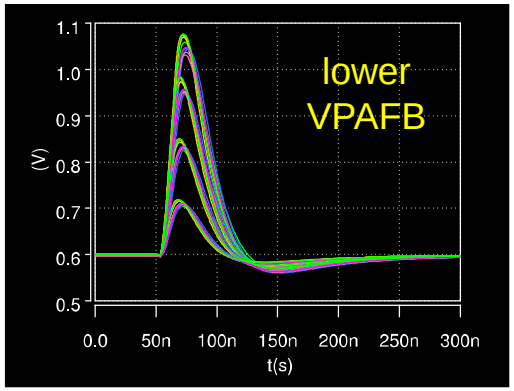
Gain Amplifier feedback resistor control

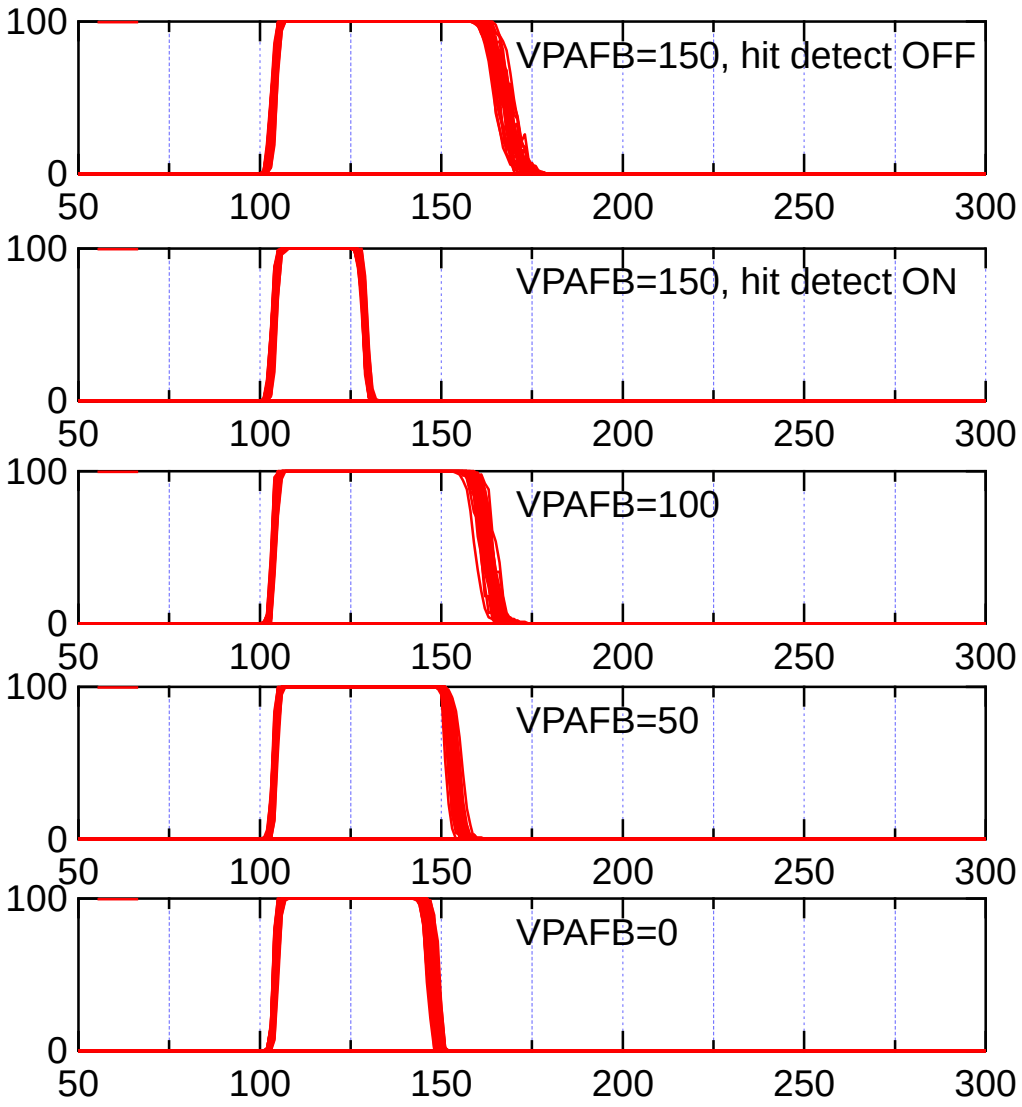
can see effect of VPAFB using
test pulse sweep - smaller values give
shorter pulse length

hit detect circuit works - only single hit
in pipeline irrespective of how long comp
O/P stays high

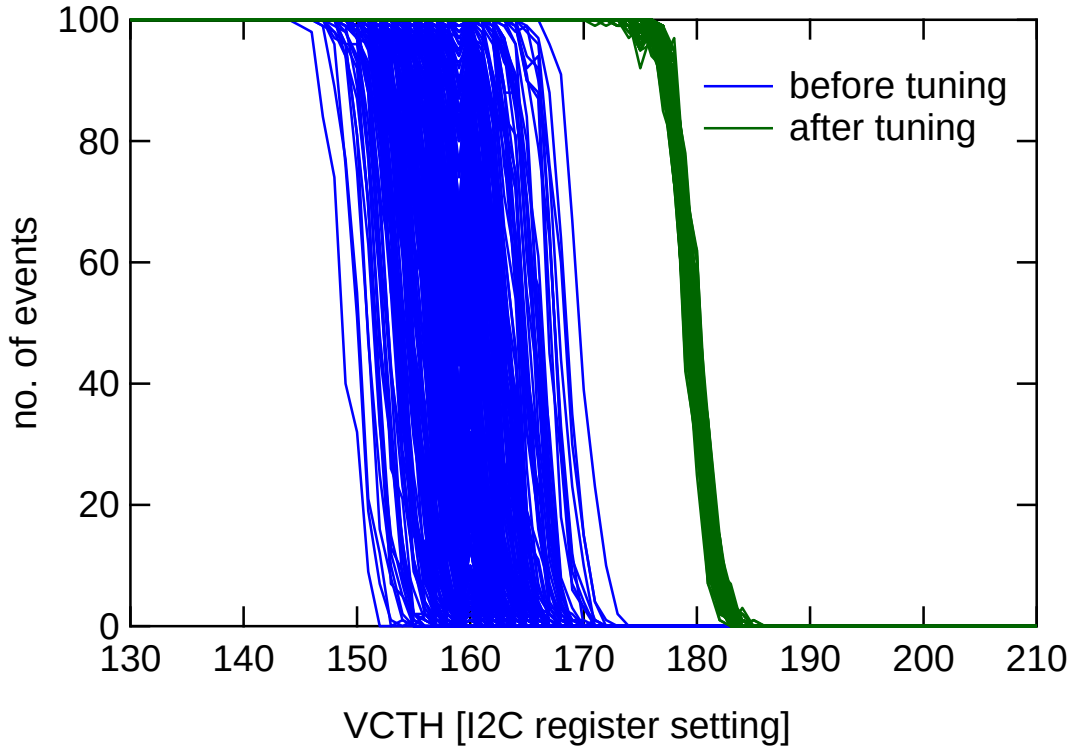
~ 2 fC signal
1 fC comp. thresh





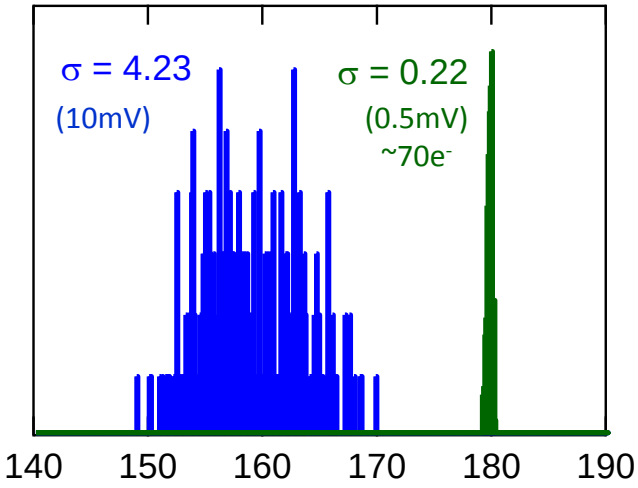


S-curves and tuning

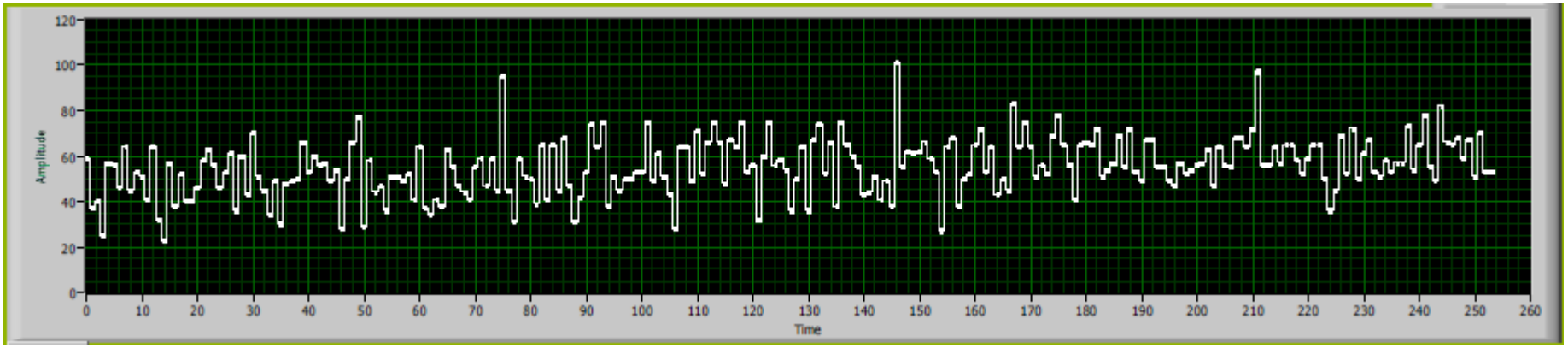


254 S-curves measured with on-chip test pulse

S-curve mid-points tuned to ~mV level



254 offset values after tuning



Stub Finding Logic

Stub finding logic

Cluster width discrimination (CWD) logic

exclude clusters with hits in >3 neighbouring channels
wide clusters not consistent with high pT track

Offset correction & correlation logic

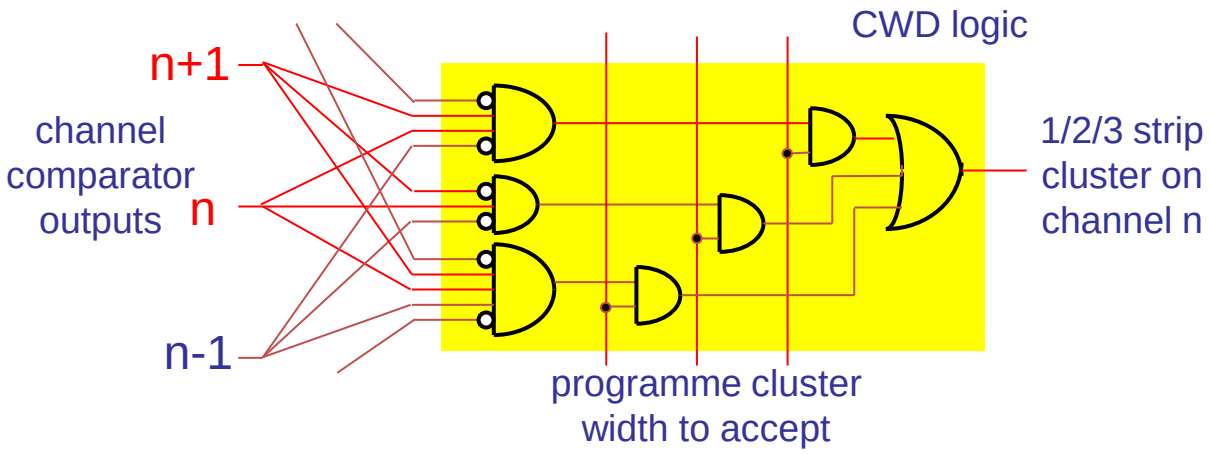
for a cluster in bottom layer, look for correlating cluster occurring in window in top layer

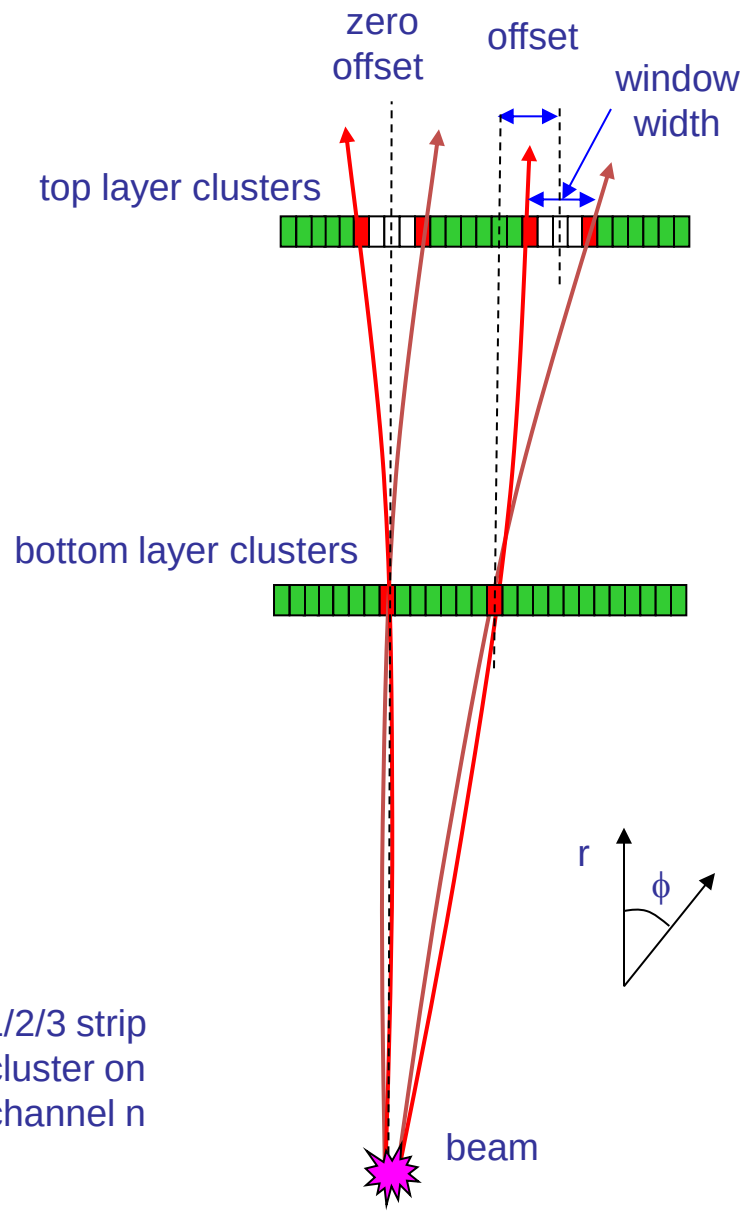
window width controls pT cut

- stub found if cluster in bottom layer corresponds to cluster within window in top layer
- programmable up to ± 8 channels

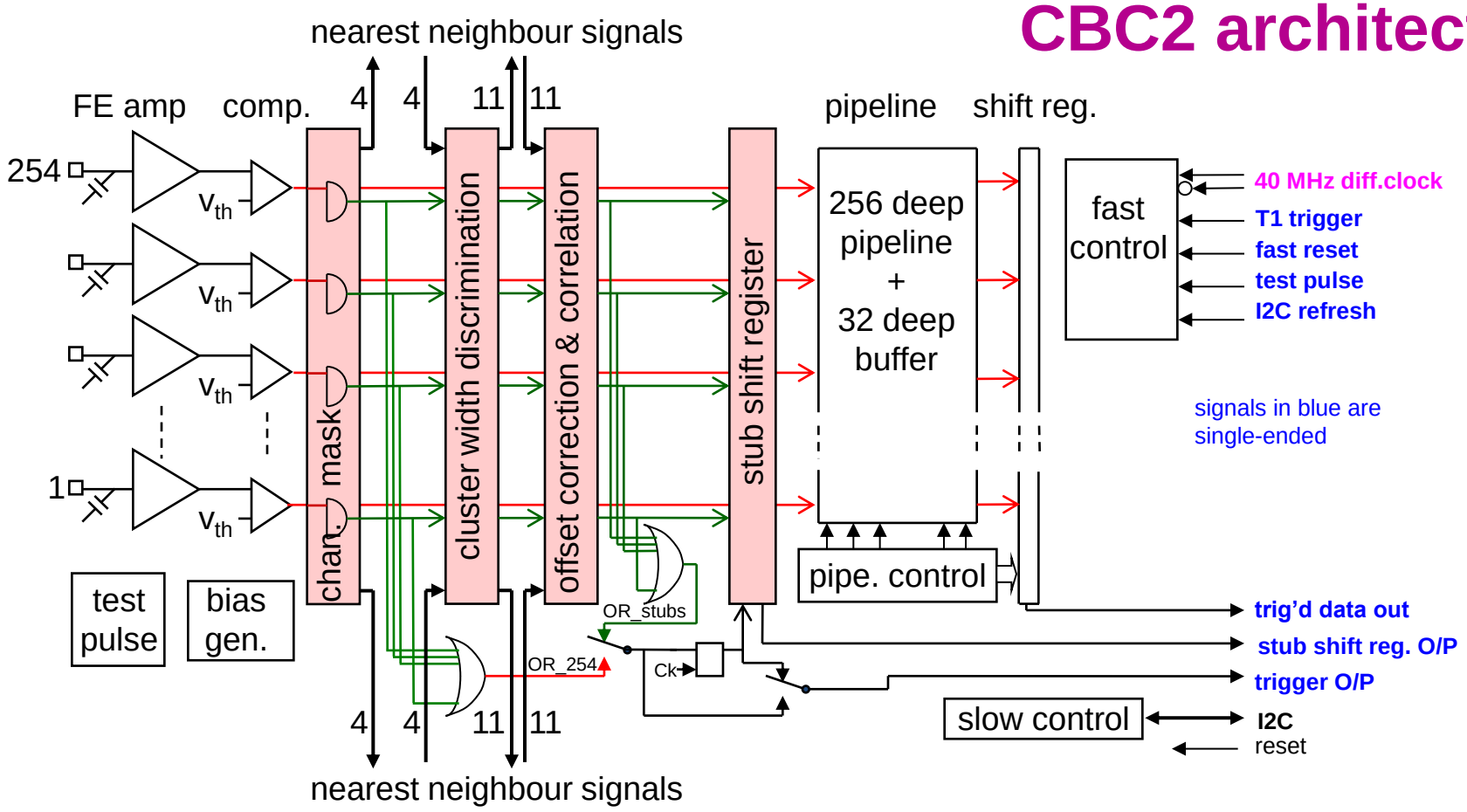
offset defines lateral displacement of window across chip

- programmable up to ± 3 channels





CBC2 architecture



254 channels: 127 from each sensor layer

test pulse: charge injection to all channels (8 groups of ~32)

channel mask: block noisy channels from trigger logic

Cluster Width Discriminator logic: exclude wide clusters >3

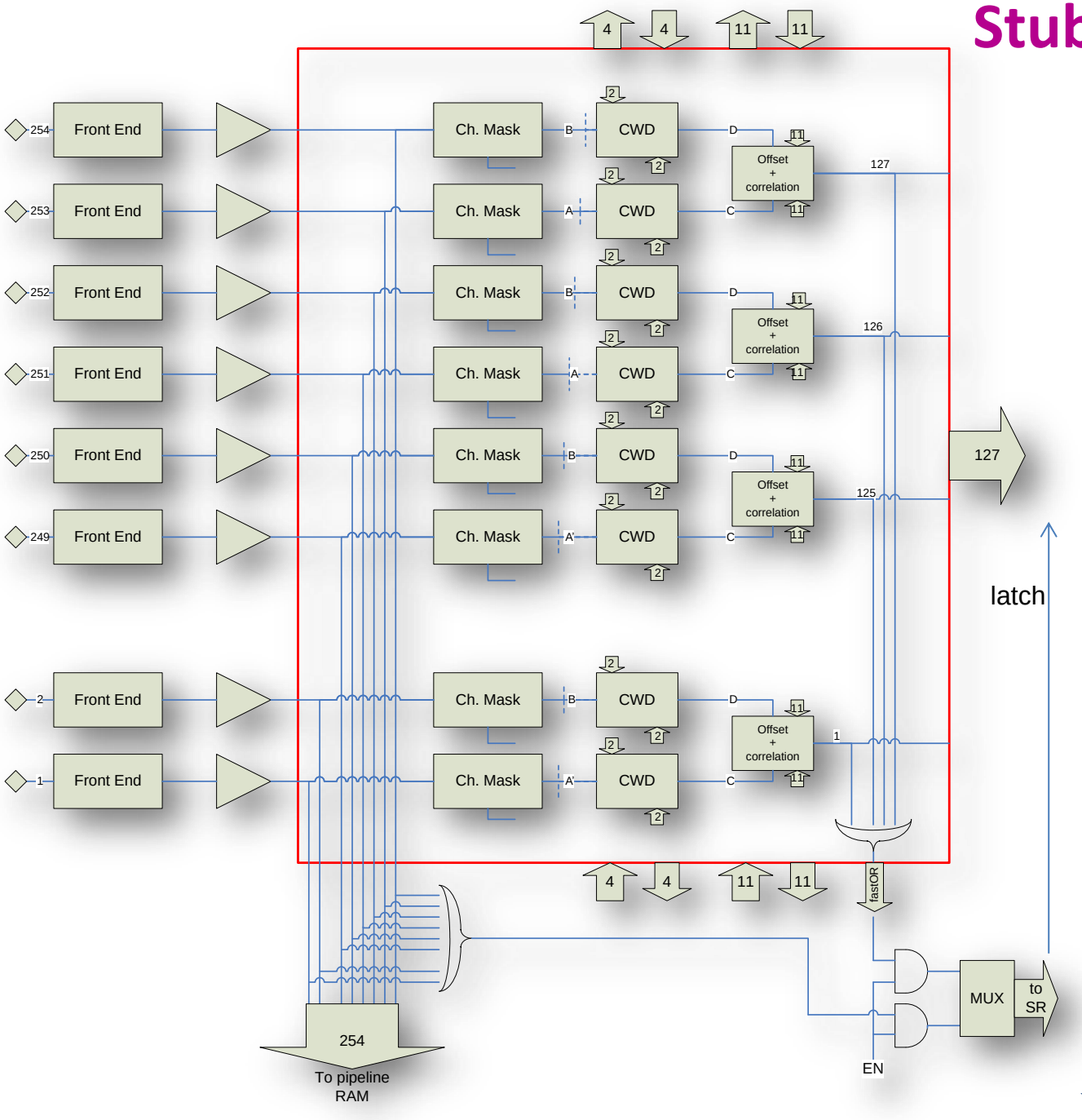
Offset Correction and Correlation logic: correct for phi offset across module and correlate between layers

trigger output: 1 bit per BX indicates stubs have been found

stub shift register: test feature - shift out result of correlation operation at 40 MHz

triggered data out: unsparsified binary data frame in response to L1 trigger

Stub finding Logic



Individual mask for noisy channels →254b from I2C reg. (can be also used to inhibit coincidence logic)

Need to be able to inhibit stub shift register operation →1b EN from I2C reg.

254-OR of channel outputs to signal any activity on chip

127-OR of stubs to control the stubs SR readout

neighbour chip signals - CWD O/Ps

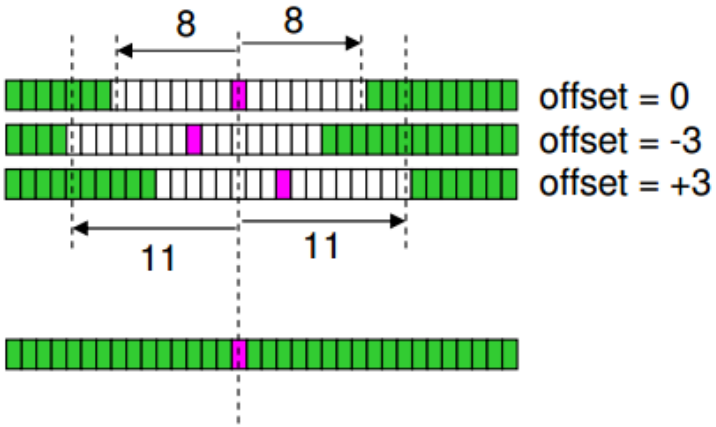
need programmability of **offset** and **window** width for upper layer channels to correlate with hit in inner layer

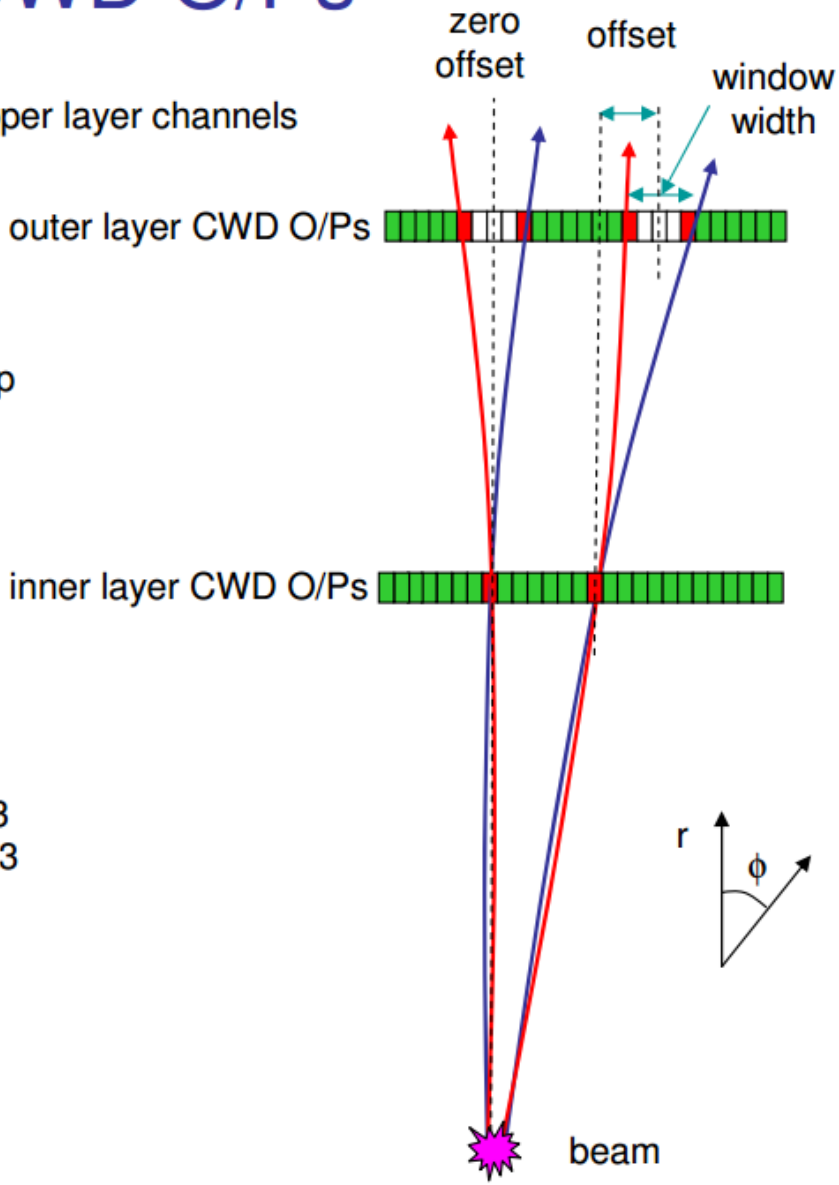
window defines Pt cut
width programmable up to **+/- 8** channels

offset defines lateral displacement of window across chip
programmable up to **+/- 3** channels

=> 11 signals to transmit to neighbouring chip
11 to receive from neighbouring chip

= 22 signals

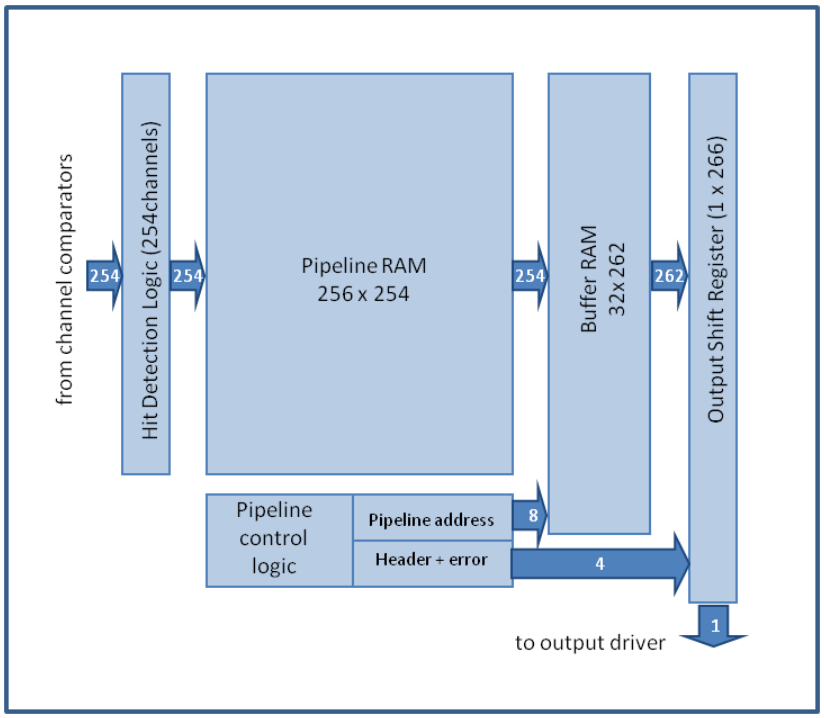




adding comp O/Ps -> 30 signals altogether, top and bottom of chip

Digital Back End: Design

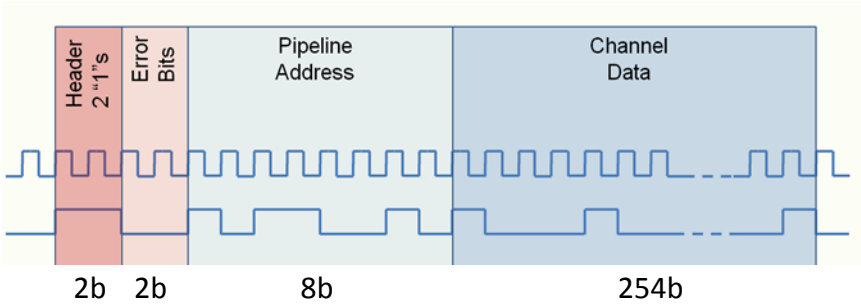
Data buffer and readout

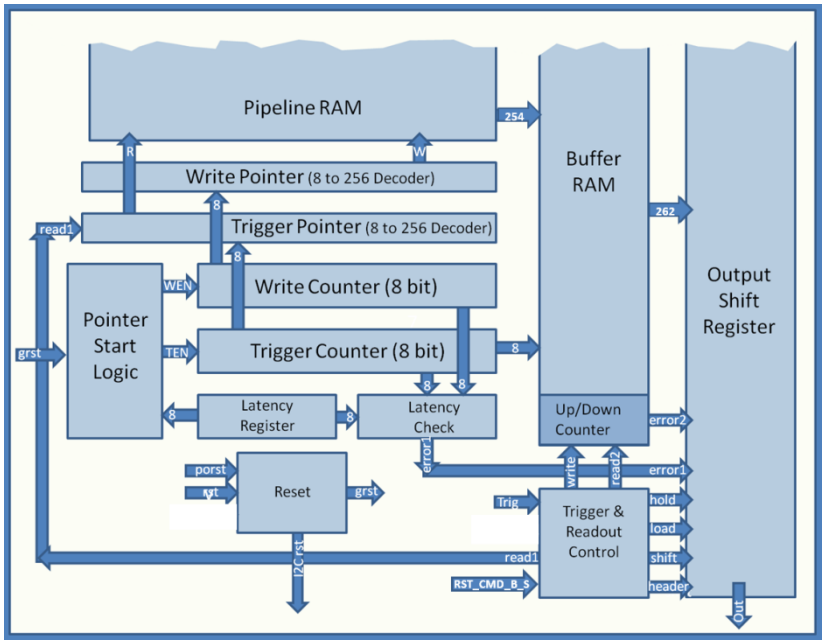


- 256-deep memory → max 6.4µs L1 trigger latency
- Dual-port SRAM (SEU tolerable for data)

- 32-deep additional buffer for events awaiting readout

- Data serialized in 266 long packets





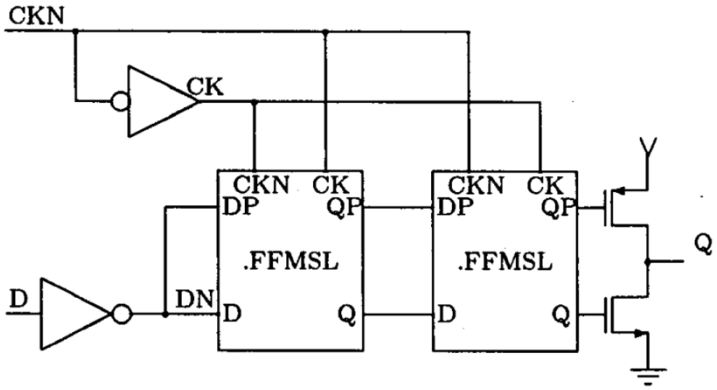
- Write and Read pointers separated by programmable latency

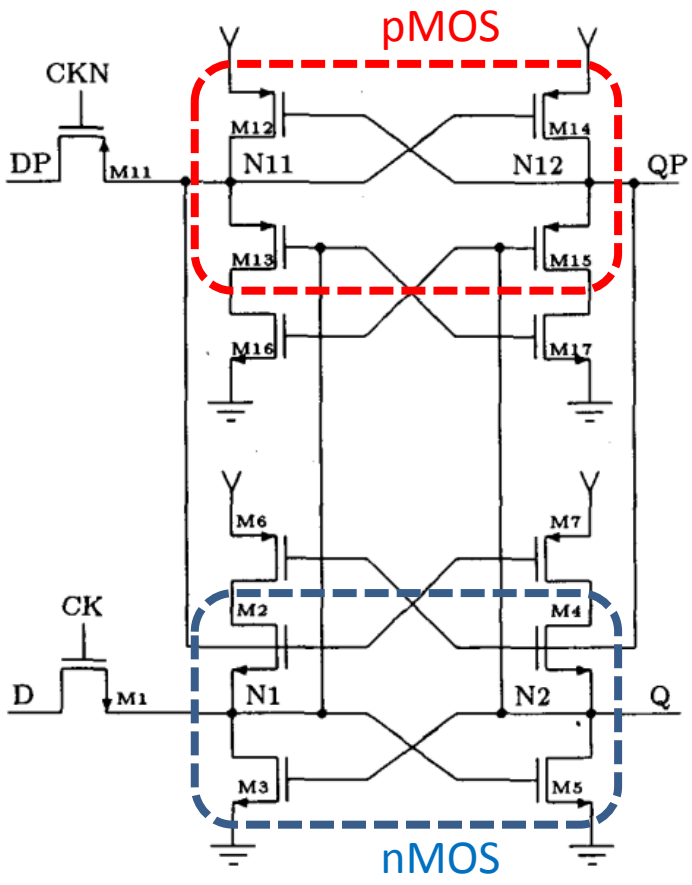
- 2 error bits:
  - Monitor the difference between Wr/Rd pointers against programmed latency
  - Buffer overflow
  - The address of the trigger counter is also a useful way to check the synchronization of different chips on the module

Liu-Whitaker SEU-hardened Flip-Flop

3 fundamental concepts:

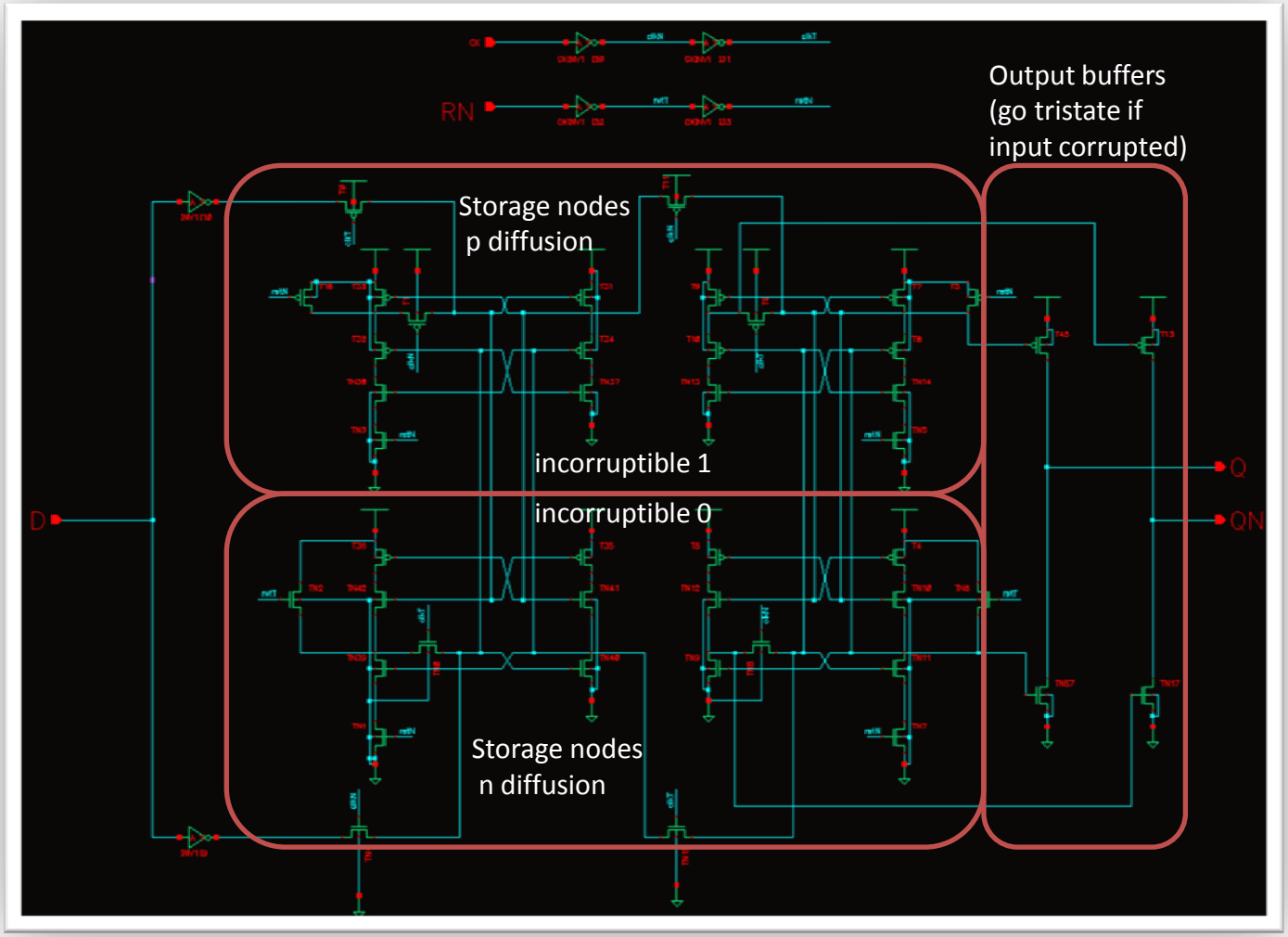
1. Redundancy
2. Restoring feedback
3. Induced current flows from n-diffusion to p-diffusion → if all pMOS transistors: inherently-hard 1; if all nMOS: hard 0





Liu, M. Norley, and Sterling Whitaker. "Low power SEU immune CMOS memory circuits." *Nuclear Science, IEEE Transactions on* 39.6 (1992): 1679-1684.

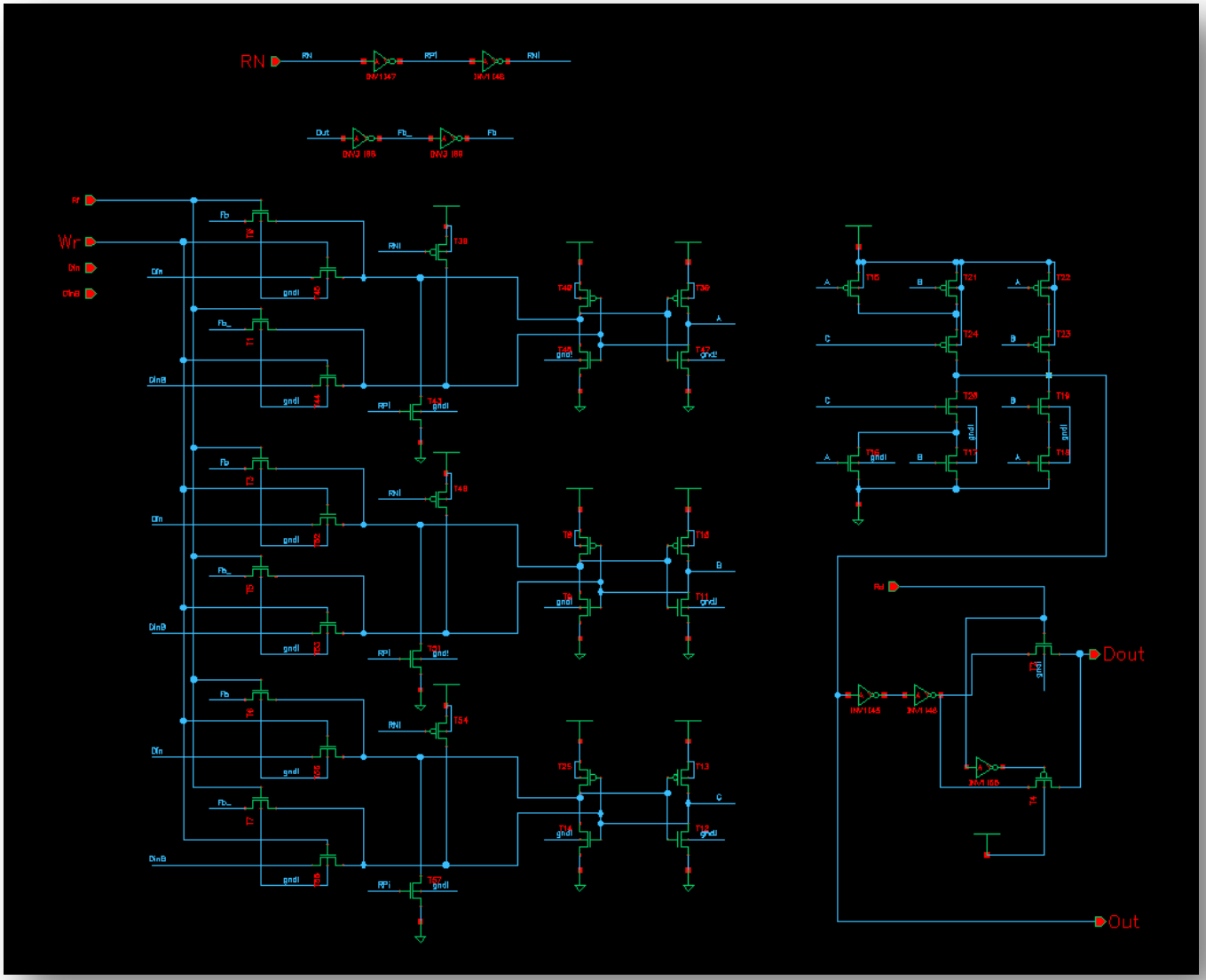
Liu-Whitaker SEU-hardened Flip-Flop (2)



Used in:

- pipeline control circuit
- Data/stub shift registers

SEU-tolerant I²C register



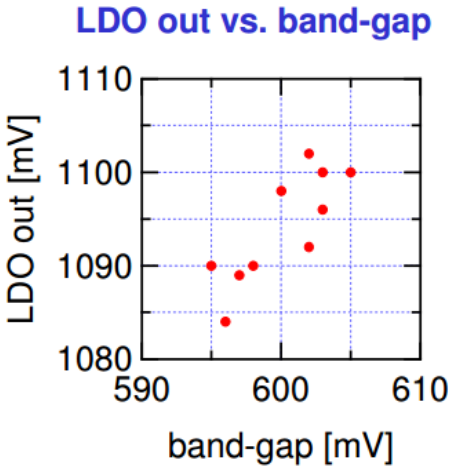
- > 300 8b I2C registers
  2page system
  - Chip modes
  - Bias settings
  - Comparator thresholds
  - Channel masks
  - …
- Triple RAM Cells with voting circuit
- Settable and resettable versions
- Can be “refreshed” by external signal to avoid cumulative errors

Power elements

Low-dropout linear regulator

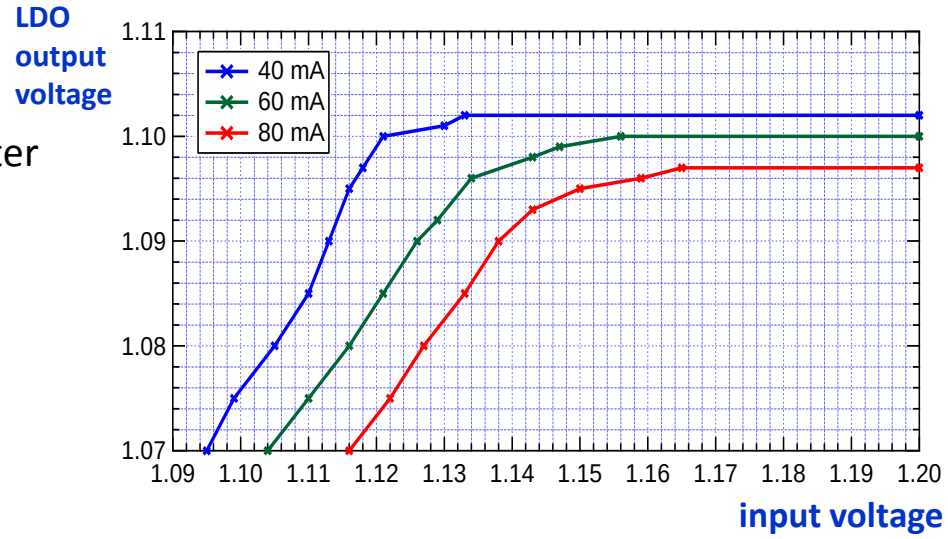
- provides clean, regulated rail to analog FE (uses CERN bandgap) ~ 1.2 Vin, 1.1 Vout
- load currents 40, 60, 80 mA
- dropouts ~ 30, 55, 70 mV (approx.)

DC shift due to series resistance (measured on wire-bonded chip)



DC-DC: (CERN)

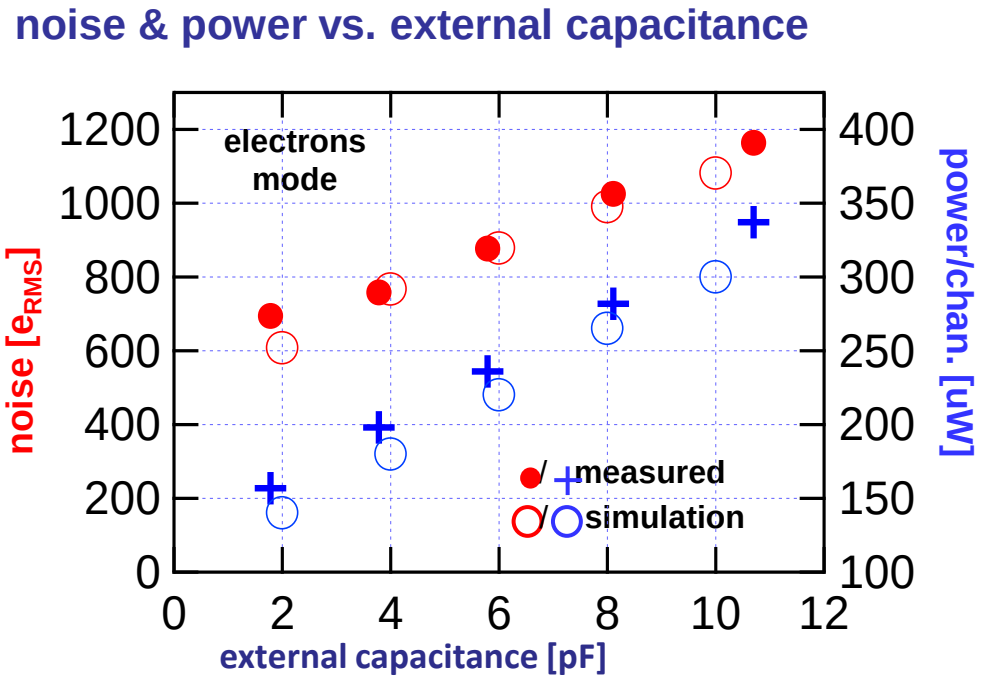
- CERN on-chip switched capacitor converter
- 2.5V → ~1.2V Can be used to power the CBC2
- Improved version wrt CBC1



M. Raymond, Imperial College

Noise & Power

Analog:	130 + (21 x C_{in}[pF]) µW
Digital:	50µW
Trig. logic:	<50µW
Total:	<230 + (21 x C_{in} [pF]) µW
APV25	~2.6mW (long strips)

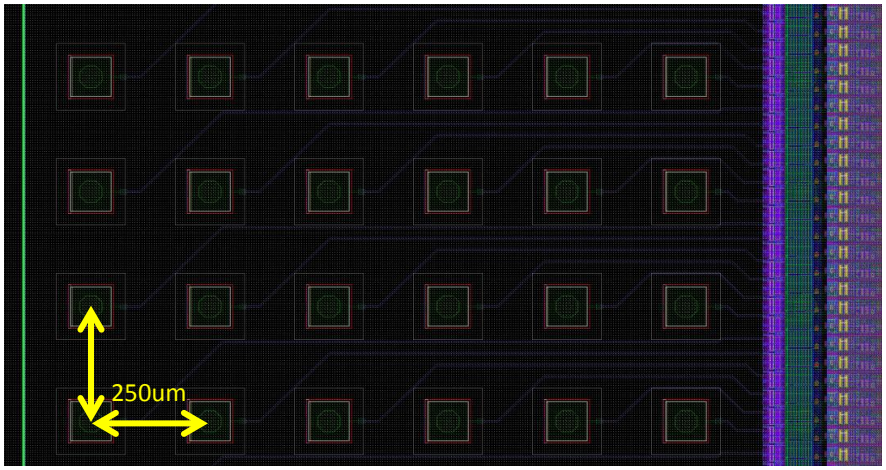


- Noise and power depends on external input capacitance
- The current settings in the front-end are adjusted to maintain the same pulse shape for different C_{in}
- Results almost identical for e^- and h^+

→ specification of **1000e^-_{RMS}** for 5cm strips met with **350µW/channel**

Layout

C4 BumpBond Pads

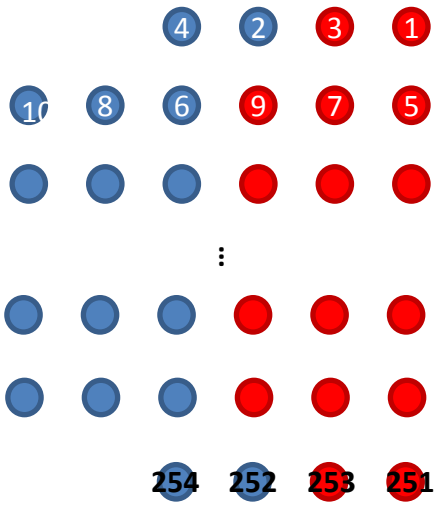


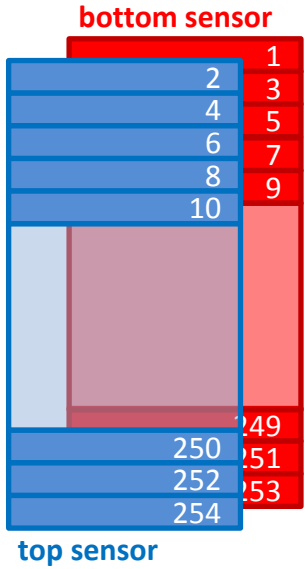
Input pads arranged in rows of 6 because of constraint in the routing of tracks on the hybrid

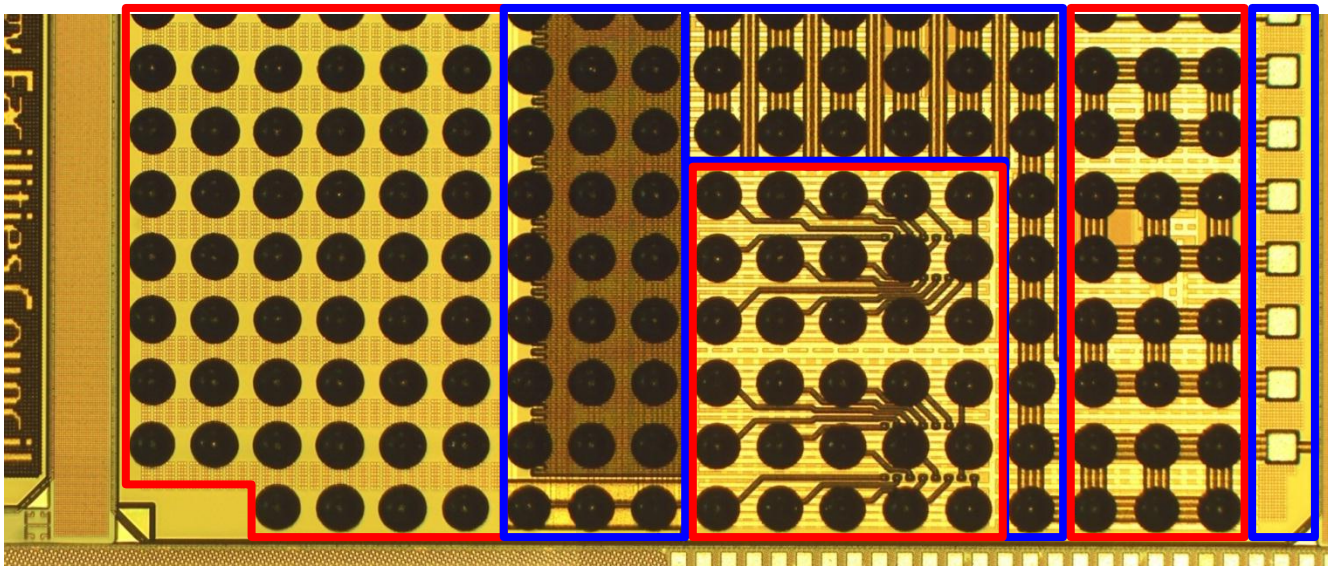
Hybrid footprint:

Inputs from top sensor

Inputs from bottom sensor



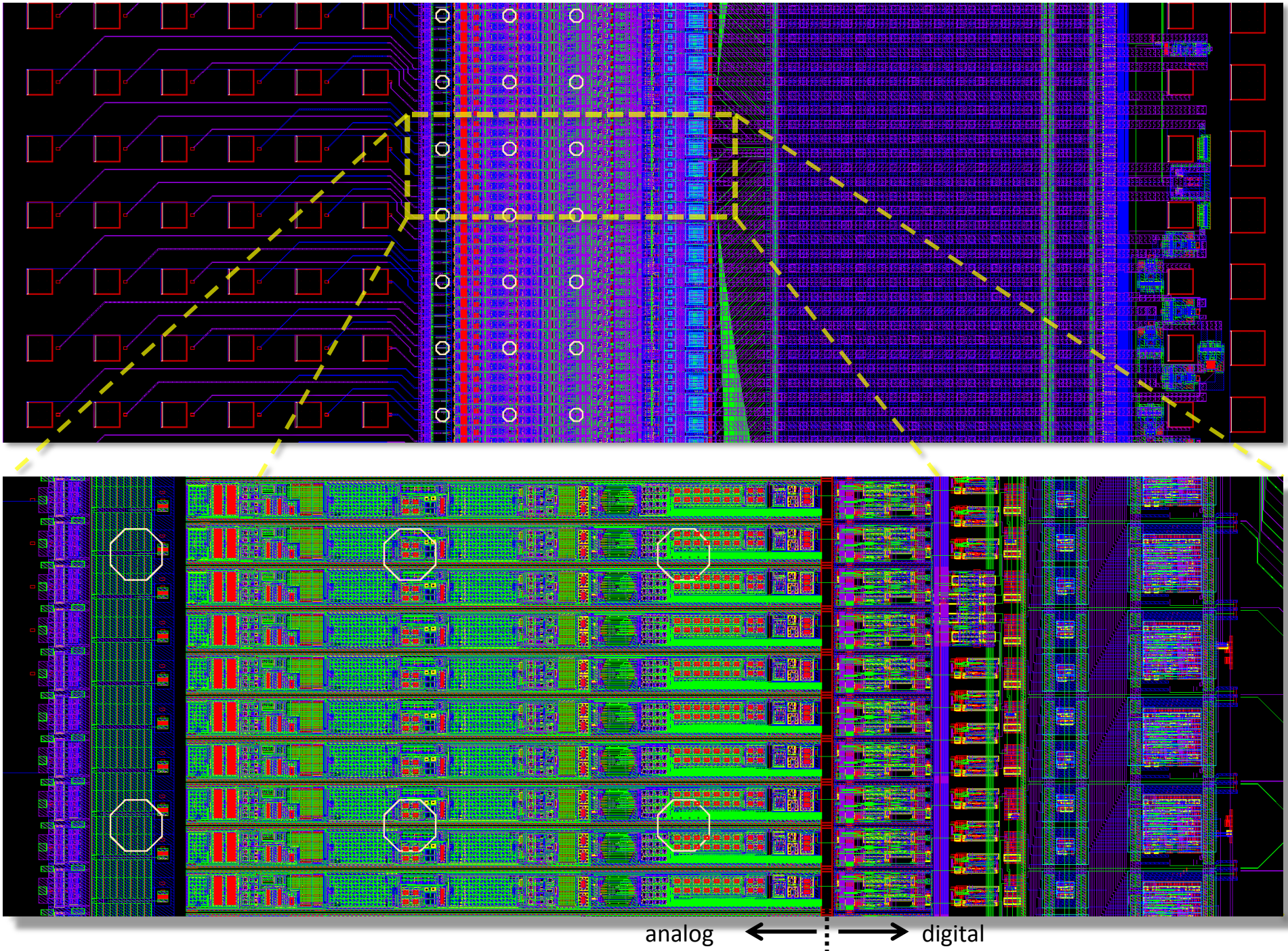




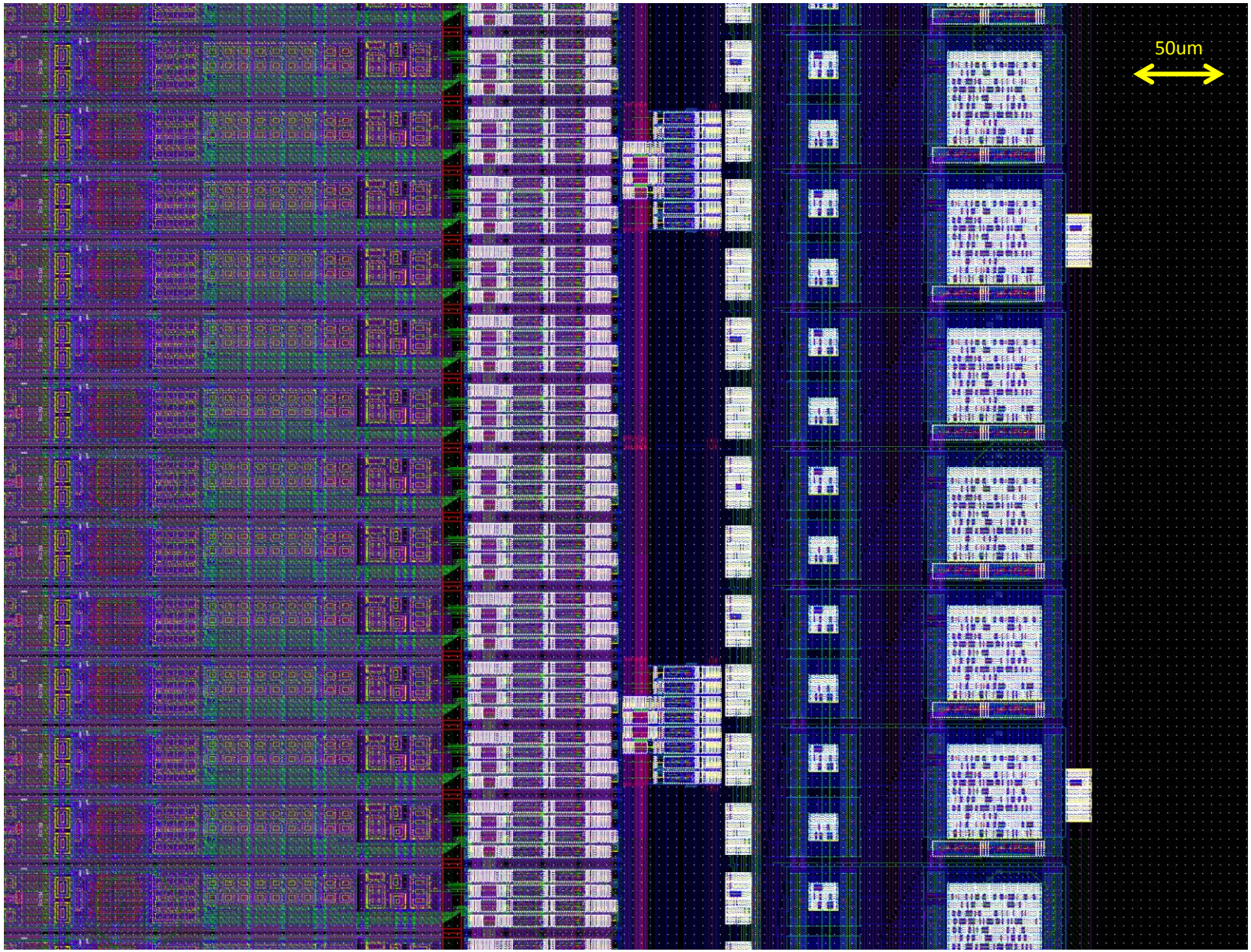
809 pads:

- Input pads
- Dummy pads
- Inter-chip pads
- Gnd pads
- I/O pads
- Wire-bonded pads

BB – WB split run

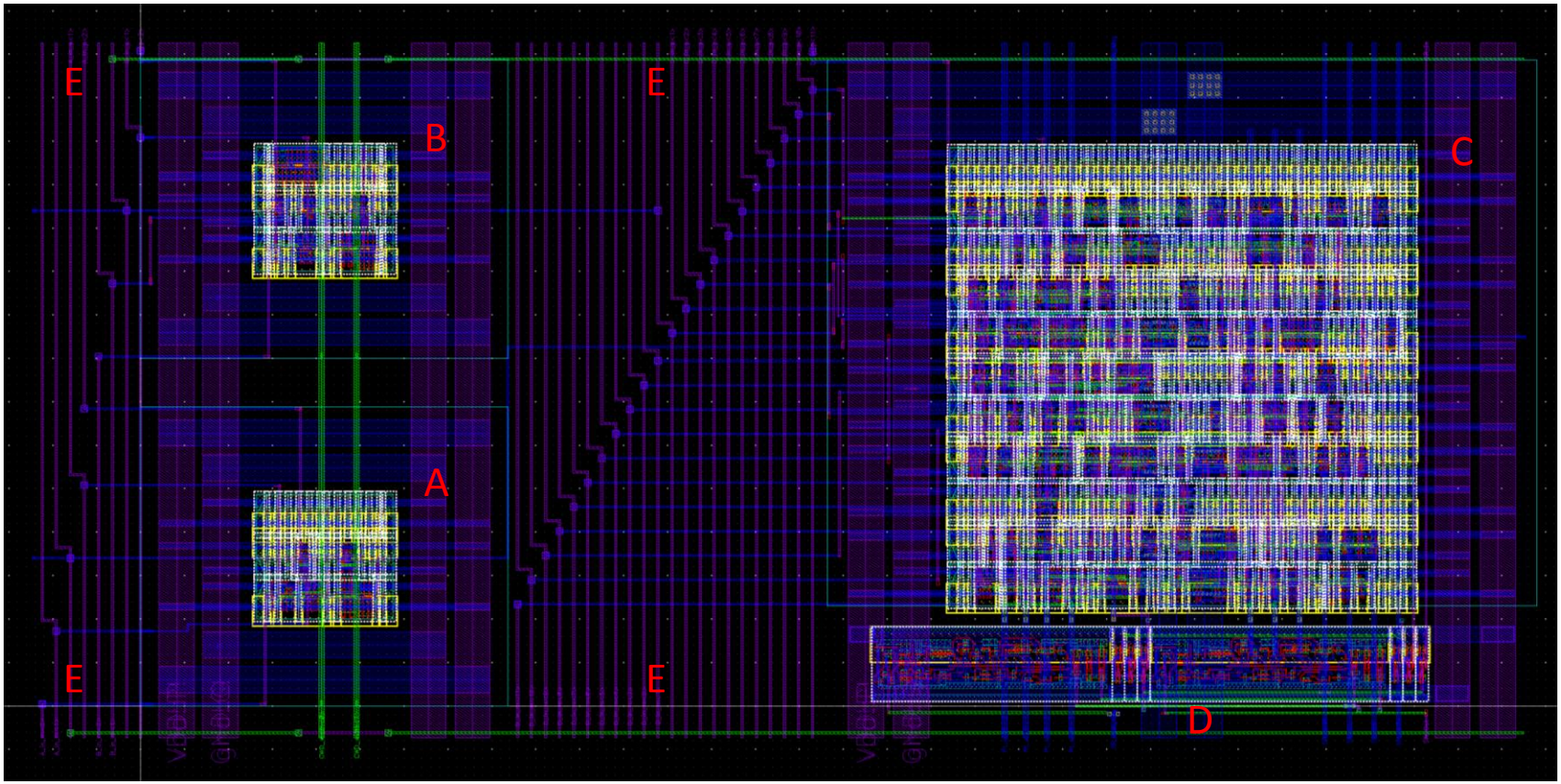

analog
digital

Digital part - Detail



Digital part - Detail

Coincidence logic - Detail



A: Cluster width discrimination for bottom sensor hits

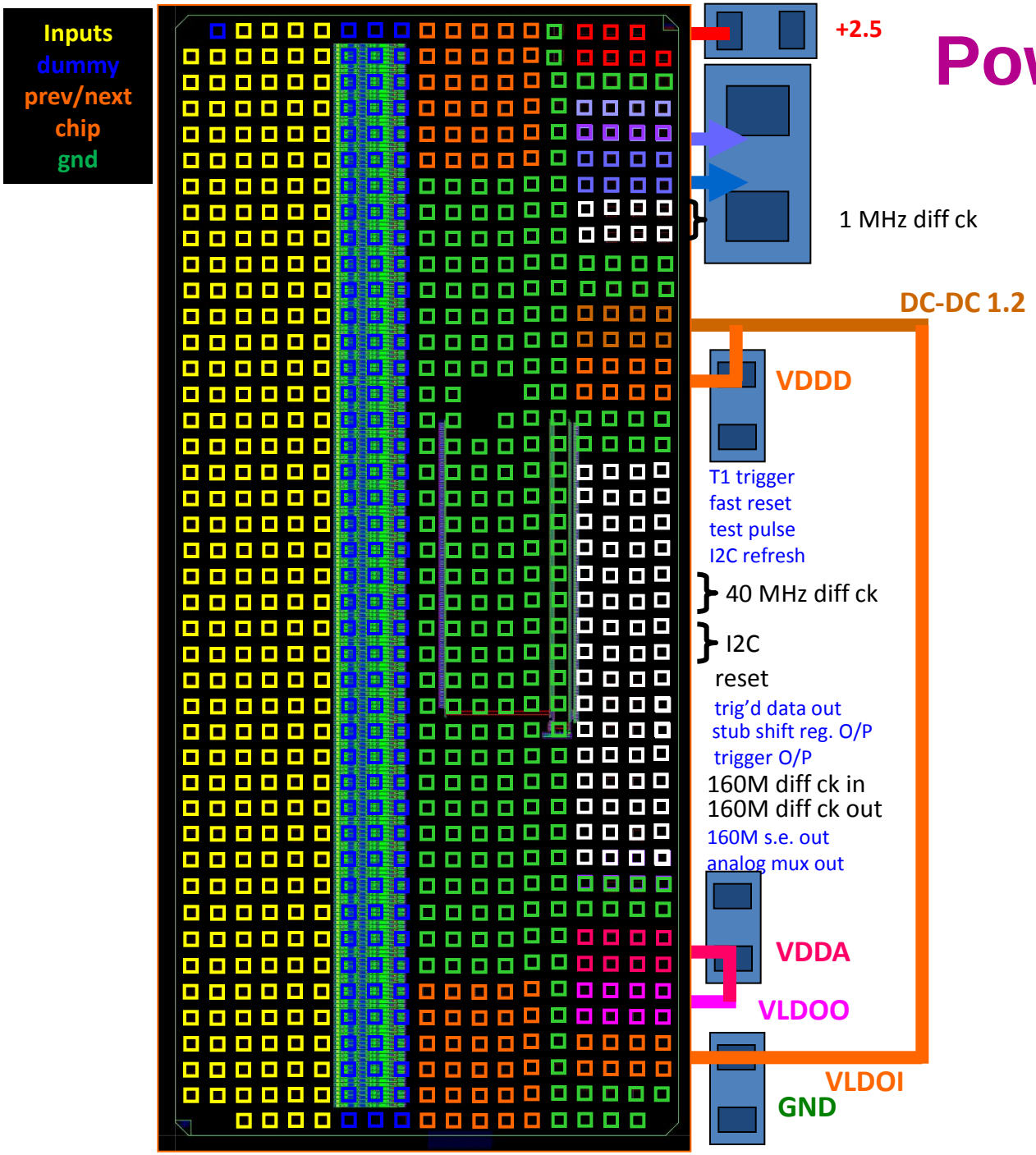
B: Cluster width discrimination for top sensor hits

C: Coincidence logic (with programmable window and offset correction)

D: Shift register for stubs readout and shadow SR for readout control

E: lines to/from previous/next channels (propagate for ~1mm (11*80um))

Power distribution



NB: the last column of PADs to the right are wire-bondable, they will not be routed on hybrid (->possible to reach the 3 pads to their left)

All but 160MHz output pads have redundancy

lines and arrows show direction of power flow (GND not shown)

note:

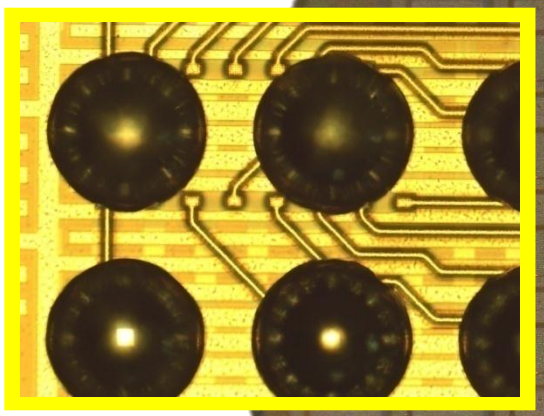
DC-DC 1.2 not connected to VDDD or VLDOI on-chip

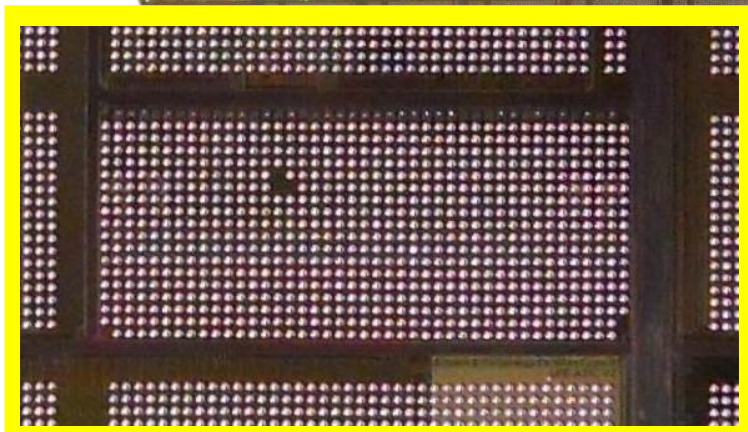
LDO output also connected to VDDA off-chip

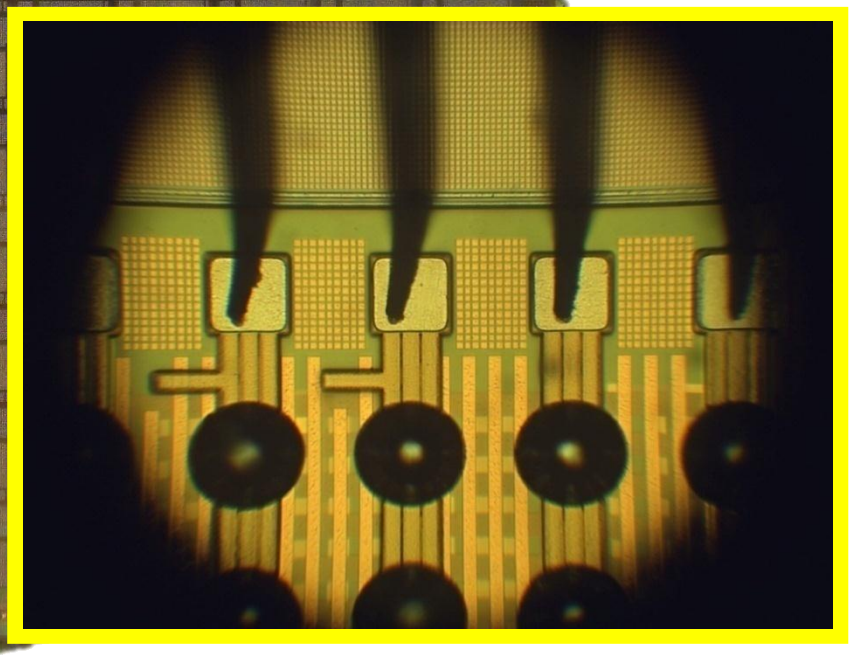
(the idea is to maximise possible effectiveness of off-chip filtering)

CBC2 C4 wafers

(shared with RAL LPD ASIC)







>97% yield

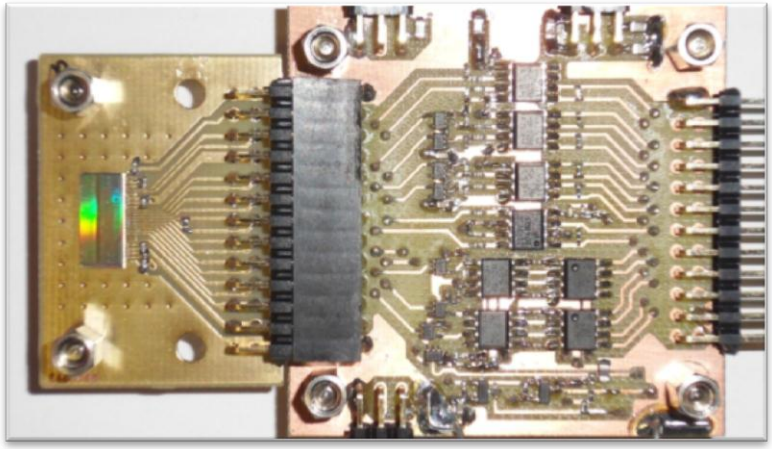
So far 2 out of 8 wafers probed (220 chips)

CBC2 Testing Activities

CBC2 testing activities

Wire-bond CBC2

- Useful to develop wafer probe procedures
- X-rays TID testing

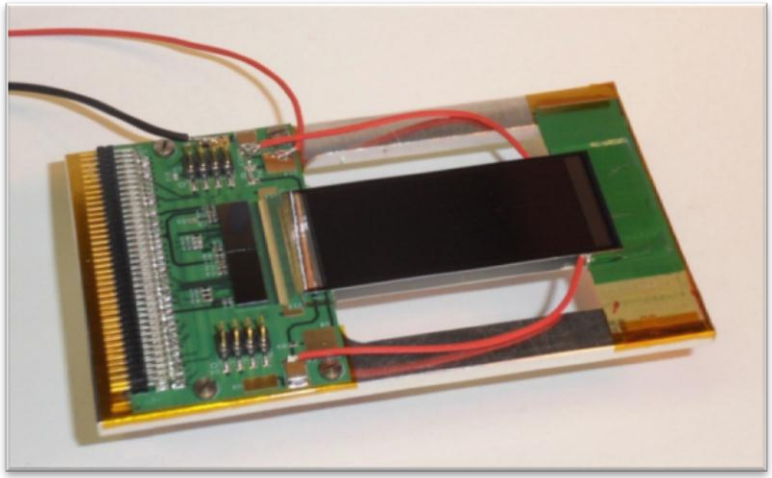


2xCBC2 hybrid

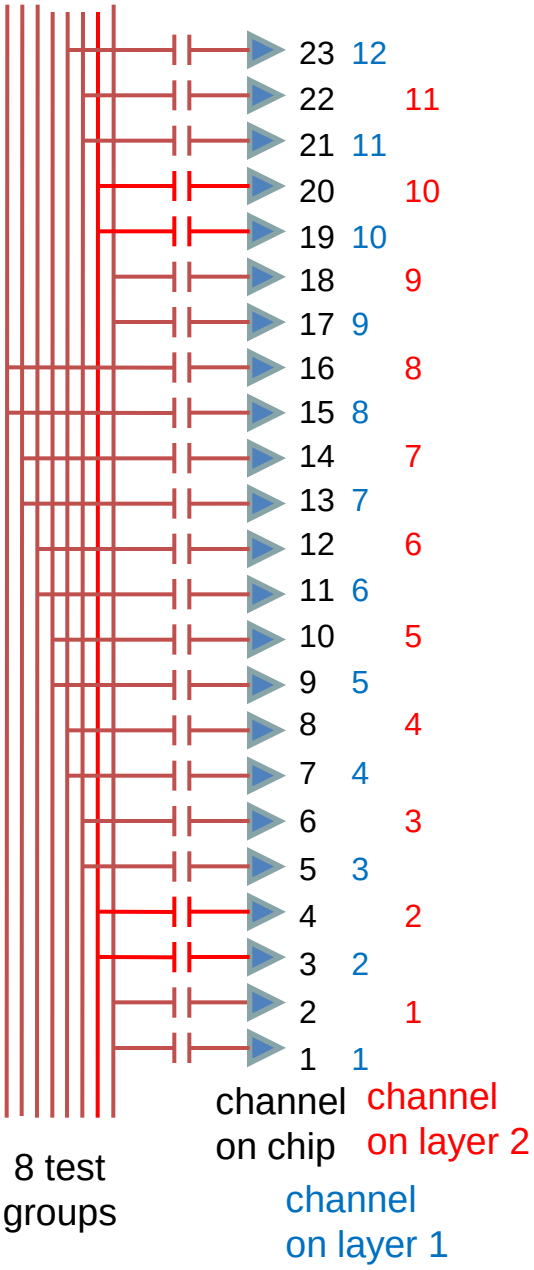
- Hybrid characterization and chip integration
- Bump-bonded ASICs
- Inter-chip links & logic

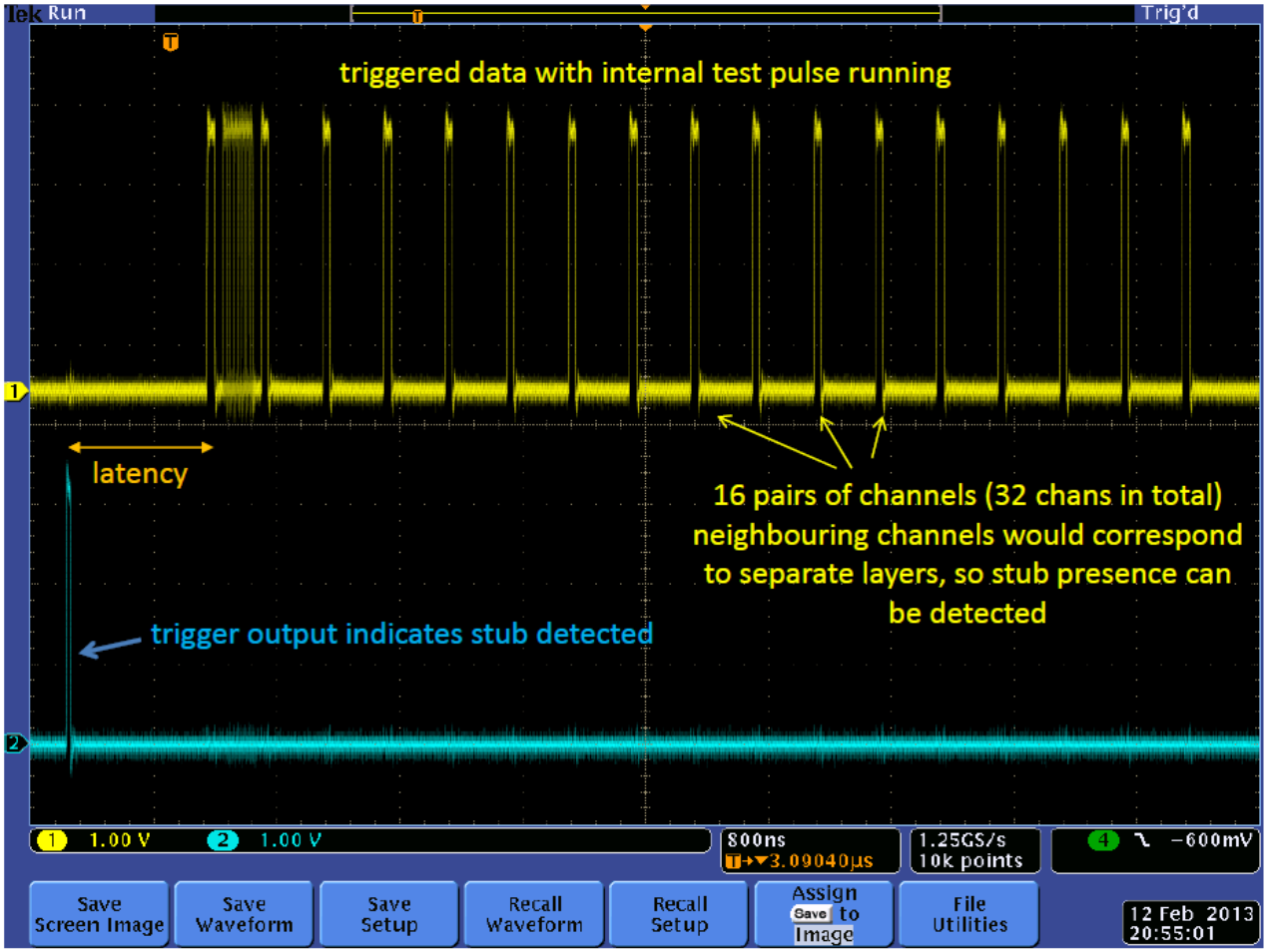
2xCBC2 mini-module + sensor

- Sr-90 source
- Cosmic rays
- Beam Test



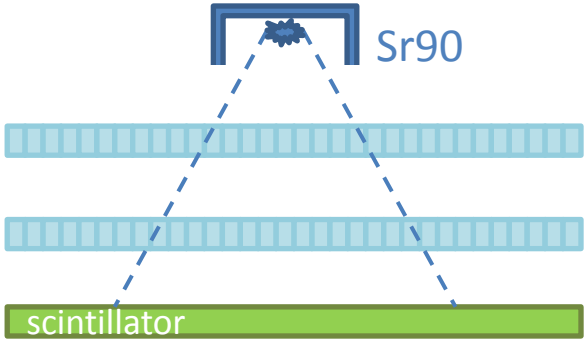
Results with test pulse

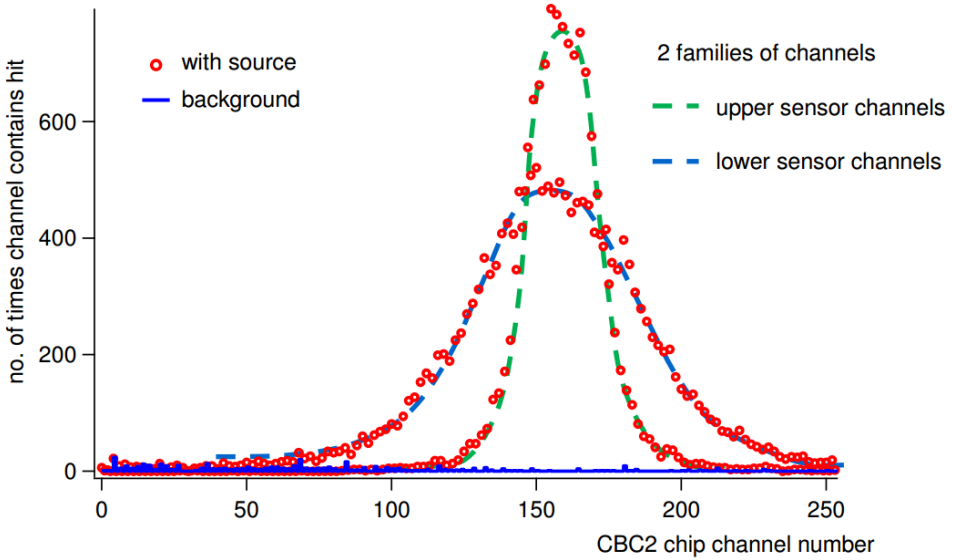


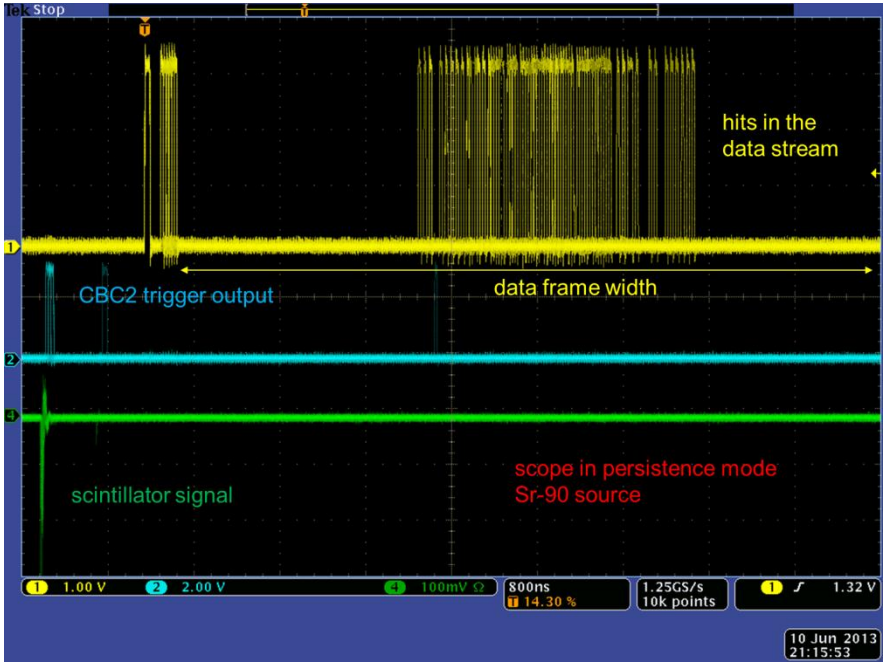


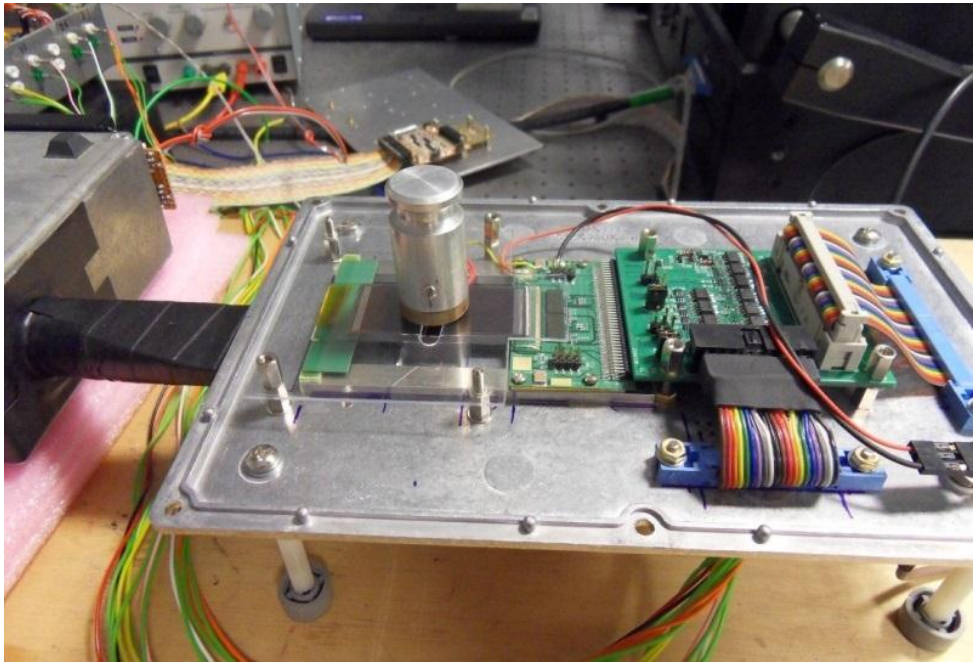
→ Test pulse together with individually-programmable channel masks can be used to fully exercise the coincidence logic

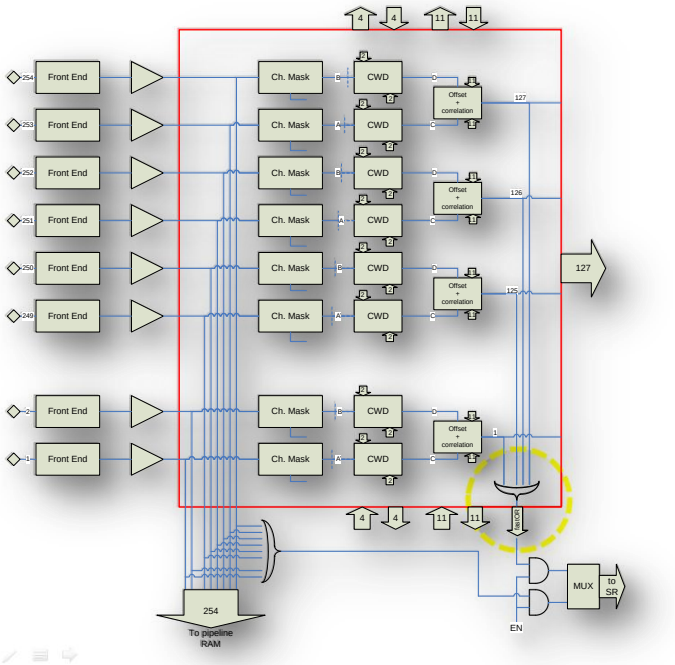
Logic tests using beta source

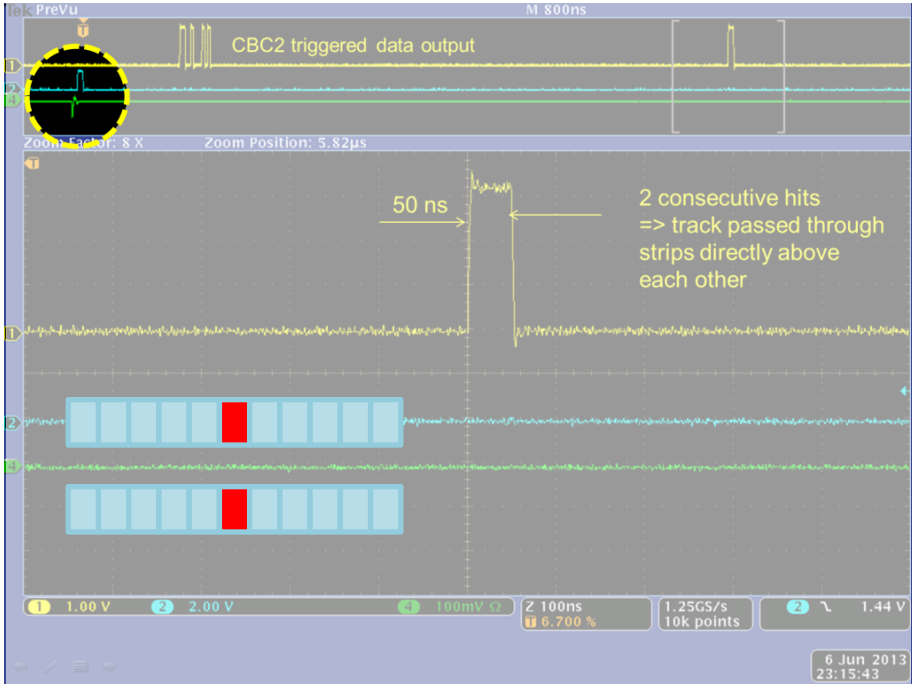


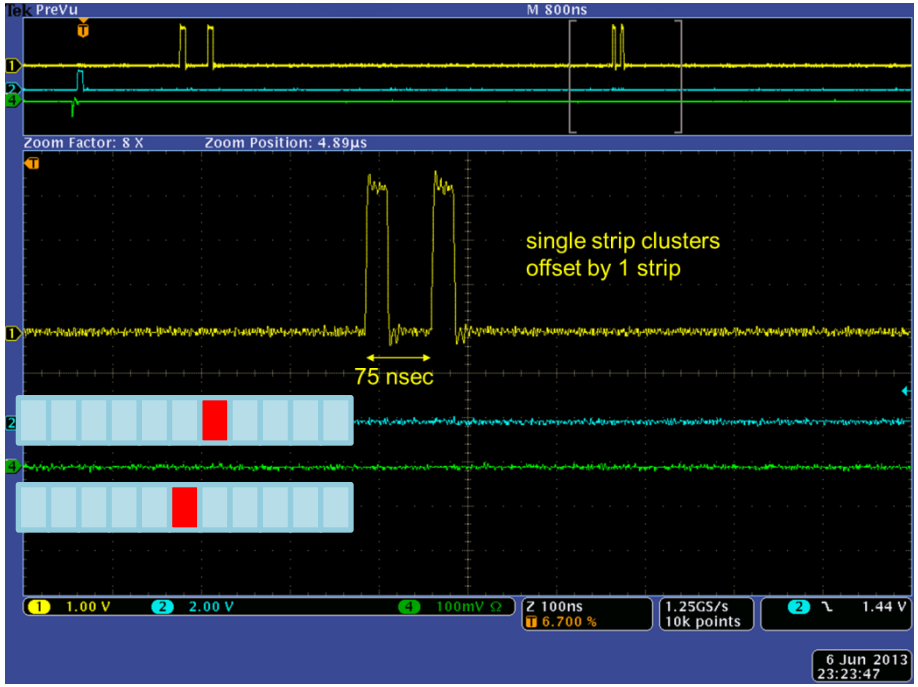


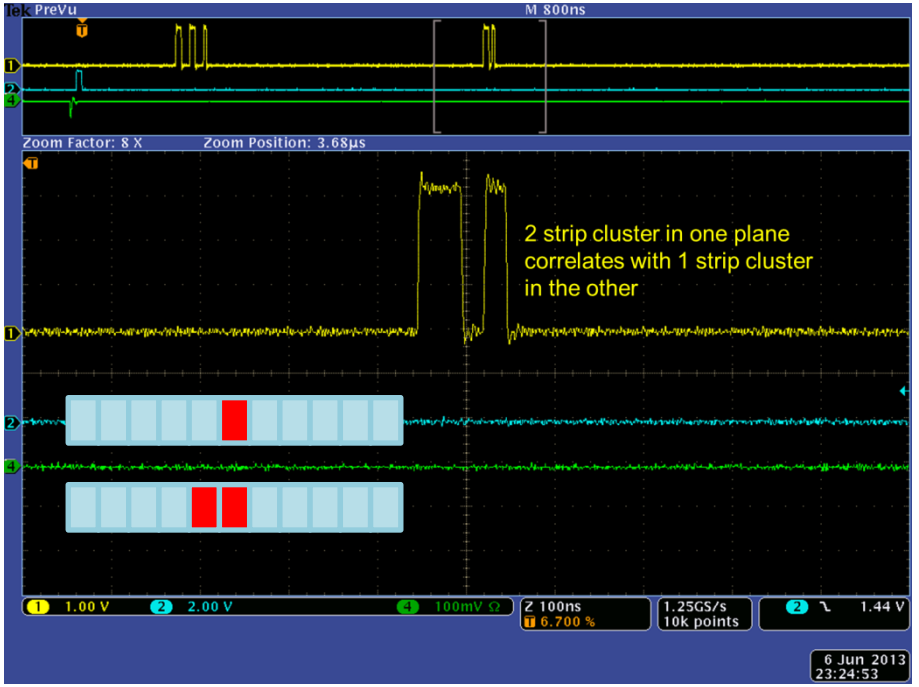




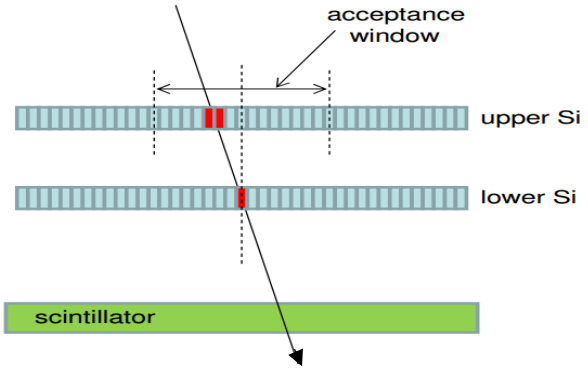

Front End
Ch. Mask
CWD
Offset + correlation
127
126
125
1
MUX
to SR
254
To pipeline RAM
EN


Tek PreVu
M 800ns
CBC2 triggered data output
Zoom Factor: 8 X
Zoom Position: 5.82µs
50 ns
2 consecutive hits
=> track passed through
strips directly above
each other
1.00 V
2.00 V
100mV Ω
Z 100ns
6.700 %
1.25GS/s
10k points
1.44 V
6 Jun 2013
23:15:43

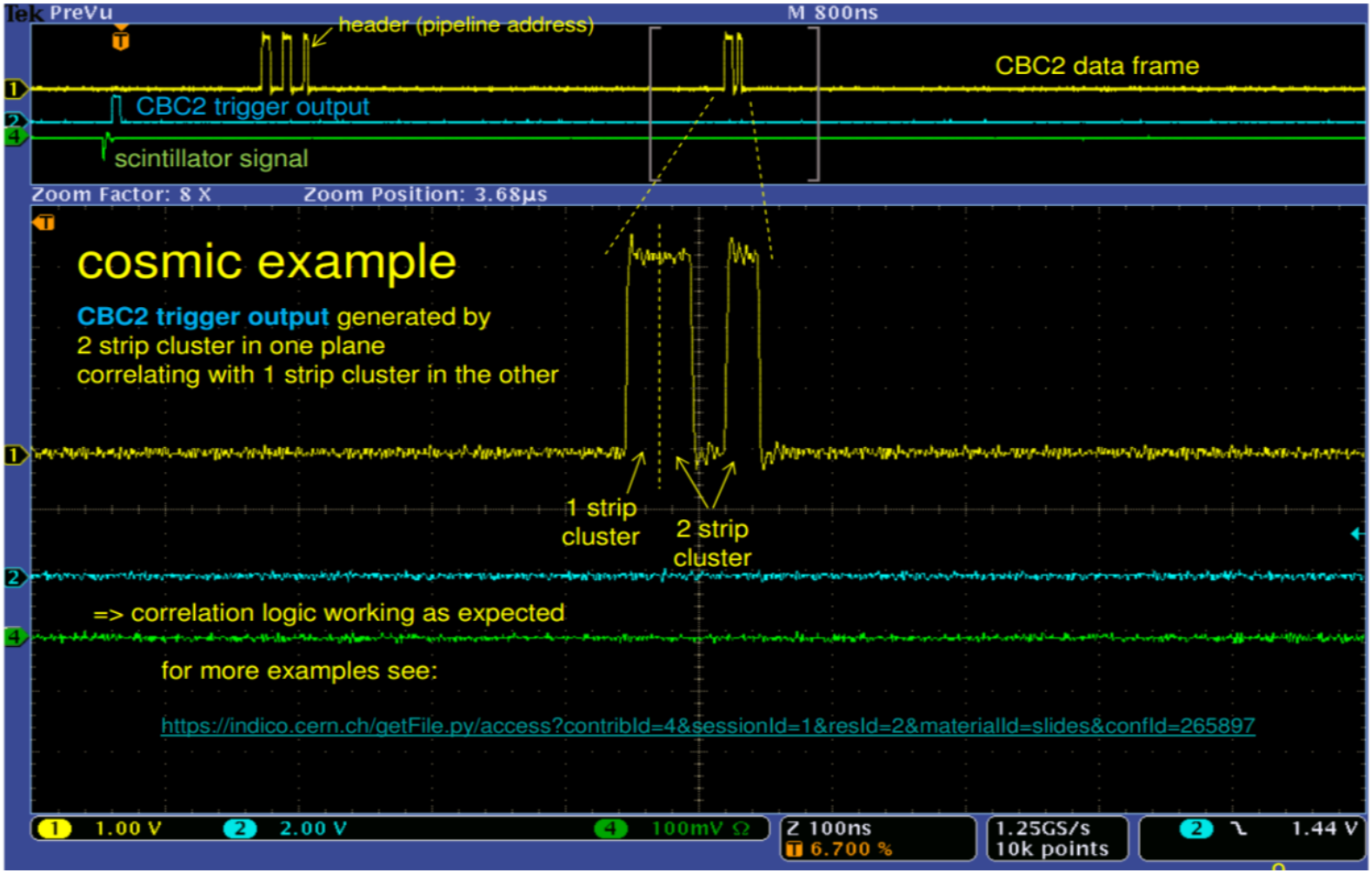

Tek PreVu
M 800ns
Zoom Factor: 8 X
Zoom Position: 4.89µs
single strip clusters
offset by 1 strip
75 nsec
1.00 V
2.00 V
100mV Ω
Z 100ns
6.700 %
1.25GS/s
10k points
1.44 V
6 Jun 2013
23:23:47


Tek PreVu
M 800ns
Zoom Factor: 8 X
Zoom Position: 3.68µs
2 strip cluster in one plane
correlates with 1 strip cluster
in the other
1.00 V
2.00 V
100mV Ω
Z 100ns
6.700 %
1.25GS/s
10k points
1.44 V
6 Jun 2013
23:24:53

Logic tests using cosmics

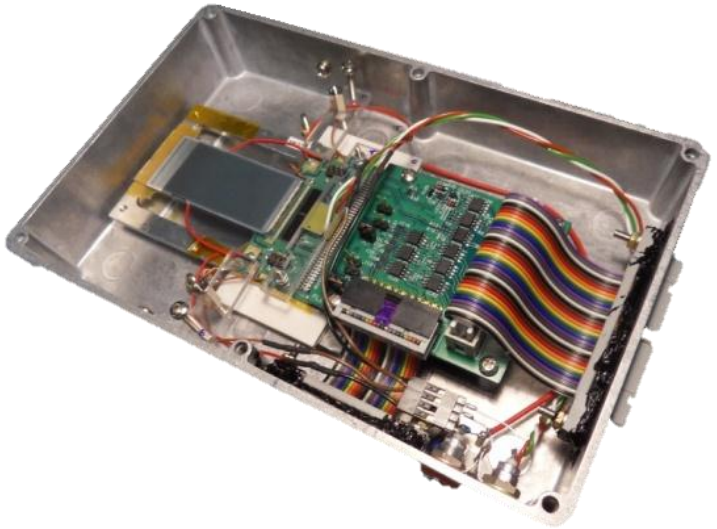


NB: very low rate (<<1Hz) even with maximum coincidence window in upper sensor

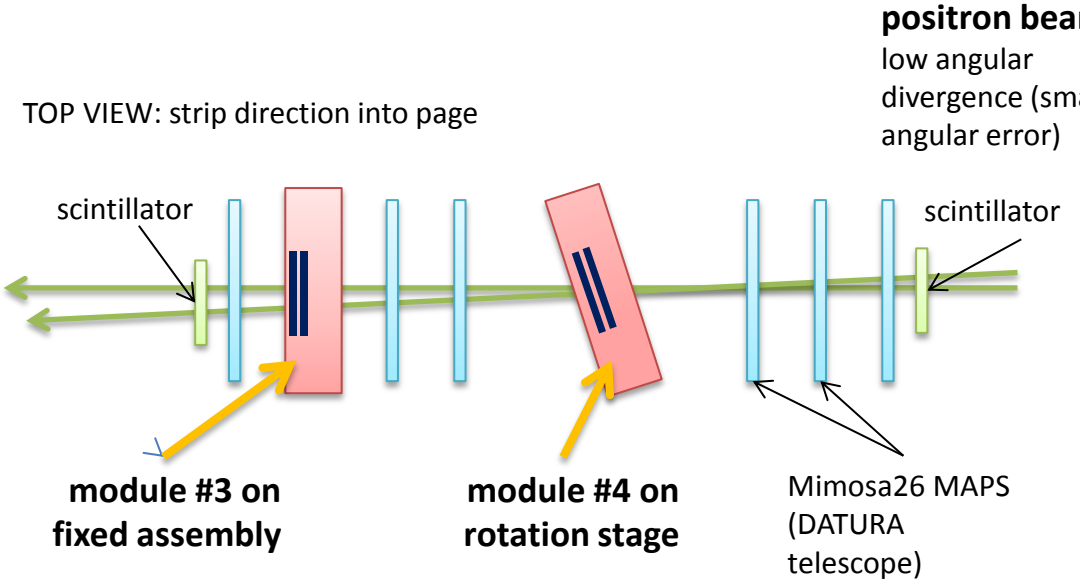


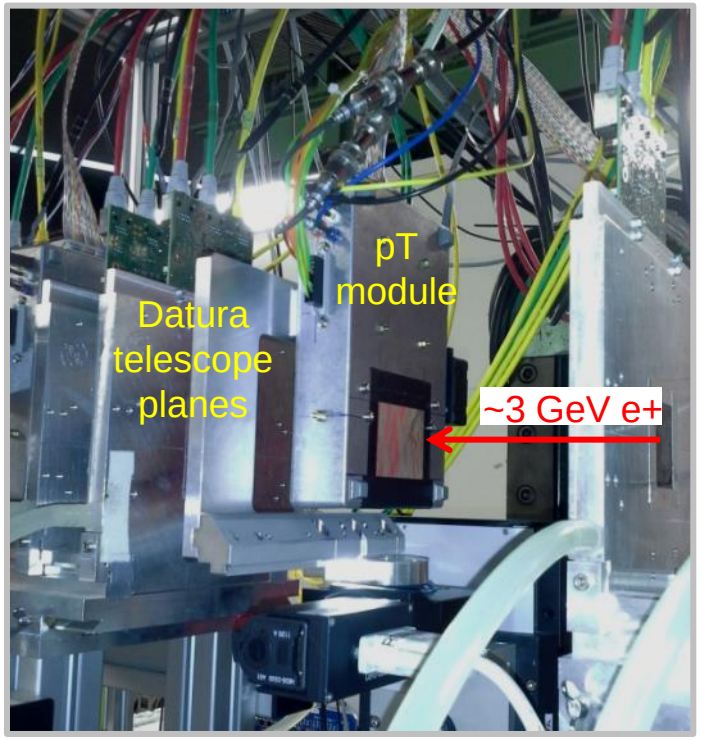
Beam Test

Pt module beam test at DESY

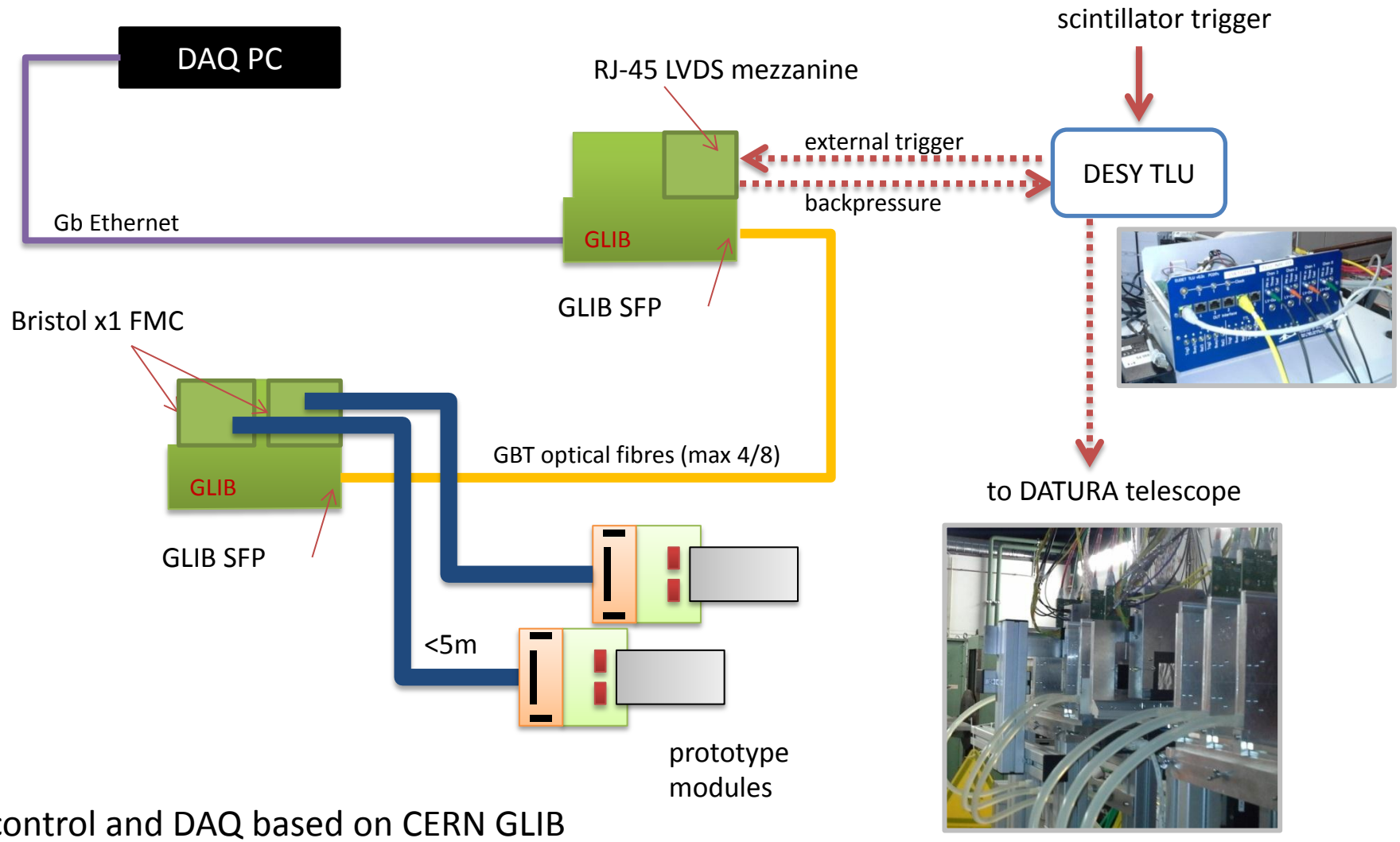


- December 2013
- 4 GeV positron beam
- Datura telescope + 2 pT modules (1 rotatable to simulate B-field effect) + 2 different strip sensors
- Custom control and DAQ





Beam test DAQ



control and DAQ based on CERN GLIB
emulating GBT functionality

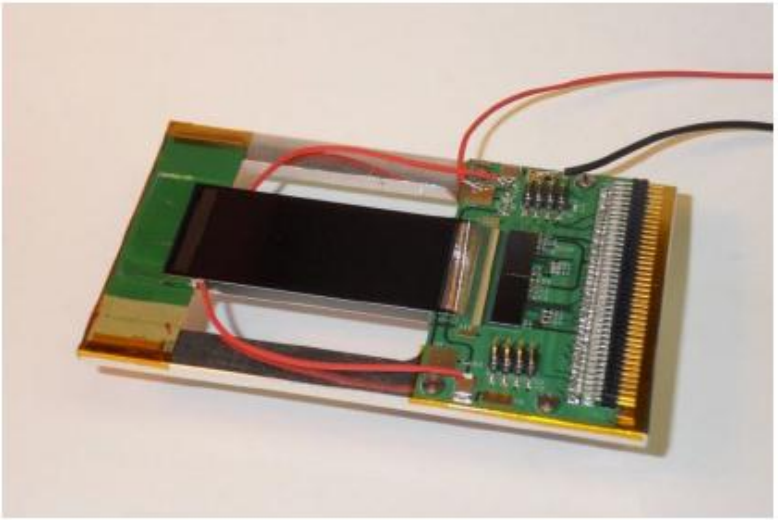
Pt modules & sensor variants

modules taken to DESY

three pt modules taken to DESY

- two different sensor types

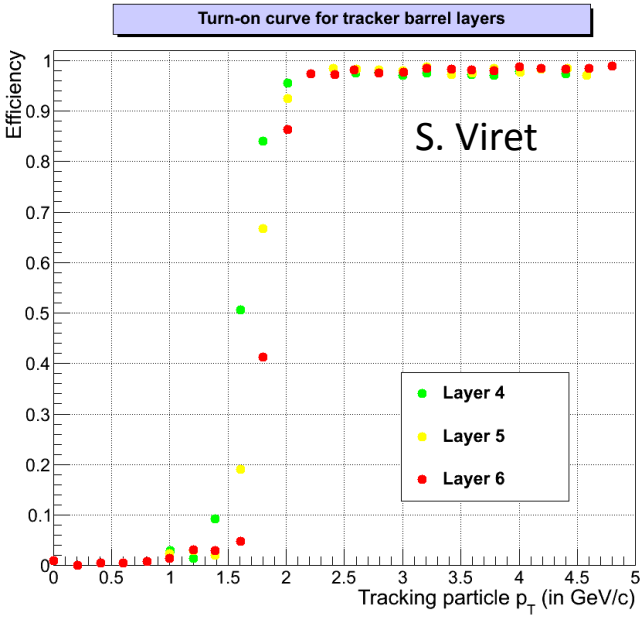
- one module left as backup

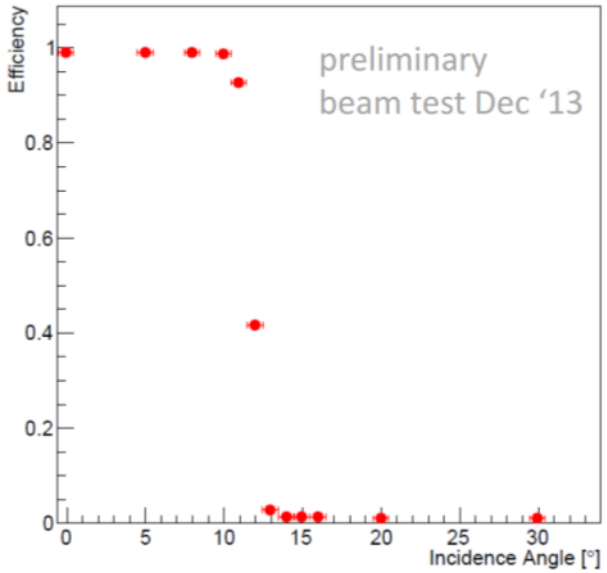


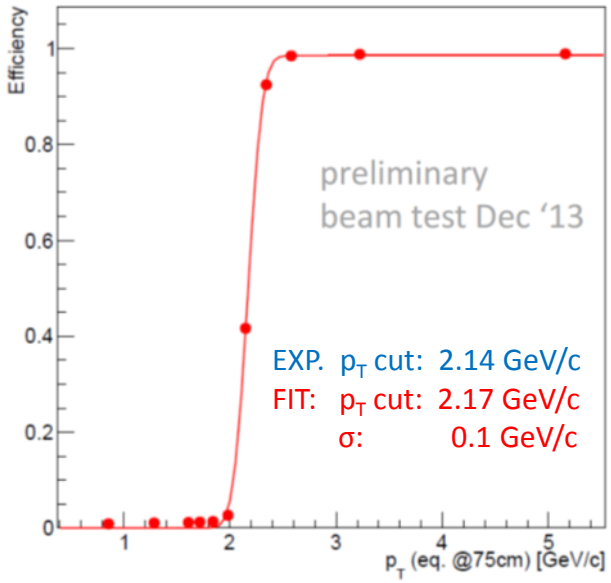
module #	sensor	sensor type	pitch [um]	thickness [um]	length [mm]	# strips	comments	tested
3	Infineon	n-type	80	300	50	256	region of disconnected channels	yes
4	CNM	p-type	90	270	54	254		yes
1	Infineon	n-type	80	300	50	256	noisy strips, disconnected channels, odd low bias behaviour	no/ backup

Beam test results

M.Pesaresi



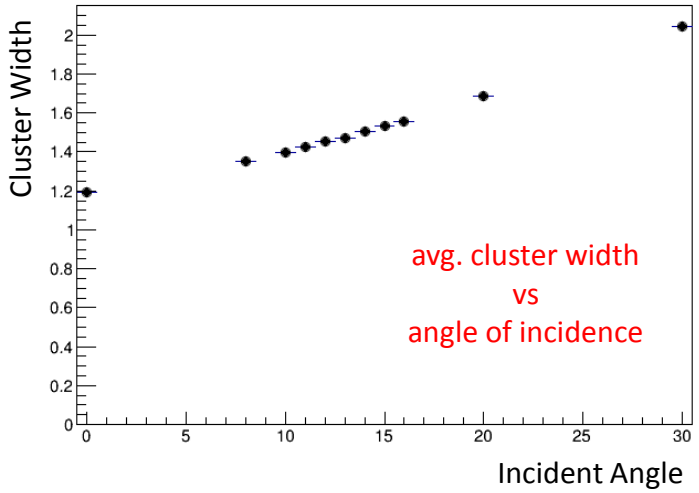




Pt Selection cut: simulation ⇨ **measured efficiency** ⇨ **reconstructed p_T cut of r=75cm layer**

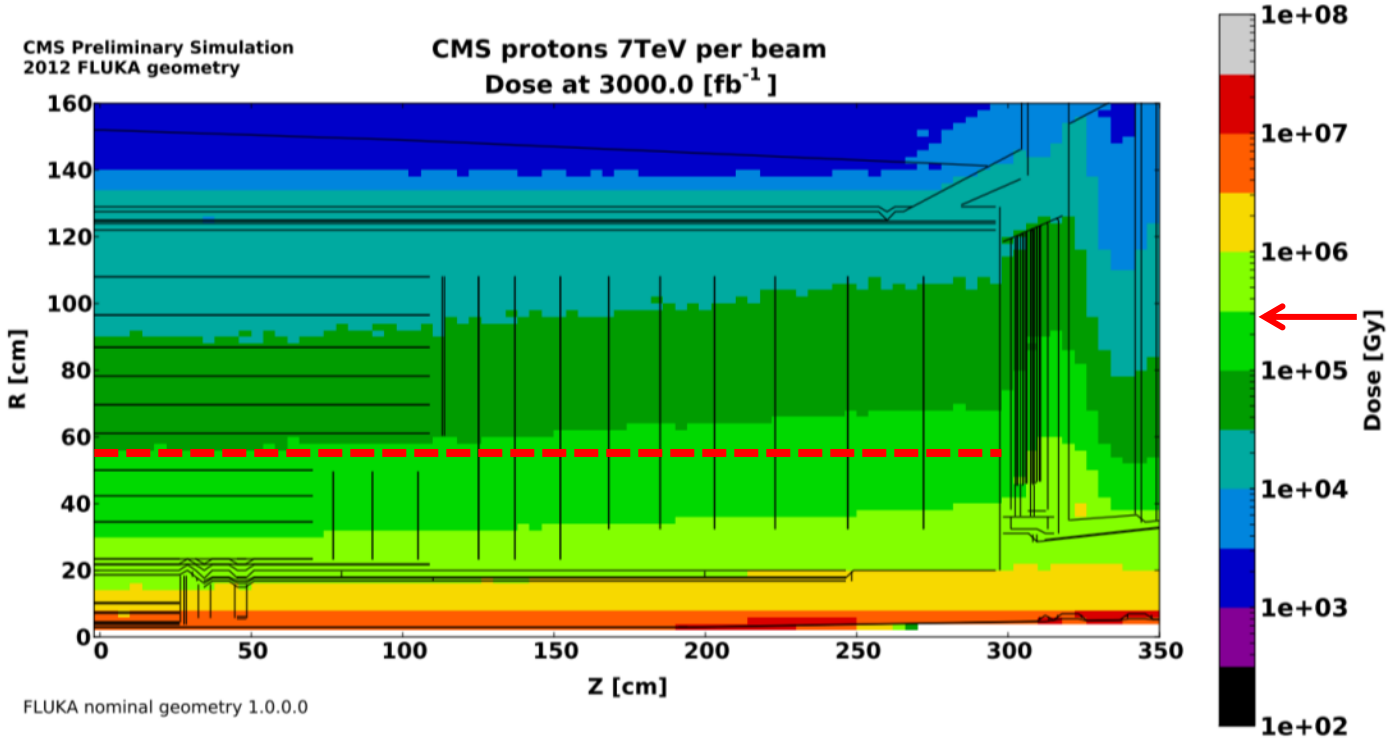
Other measurements include:

- **Study of cluster width**
- **System noise**
- **Beam profile**



Total Ionizing Dose Testing

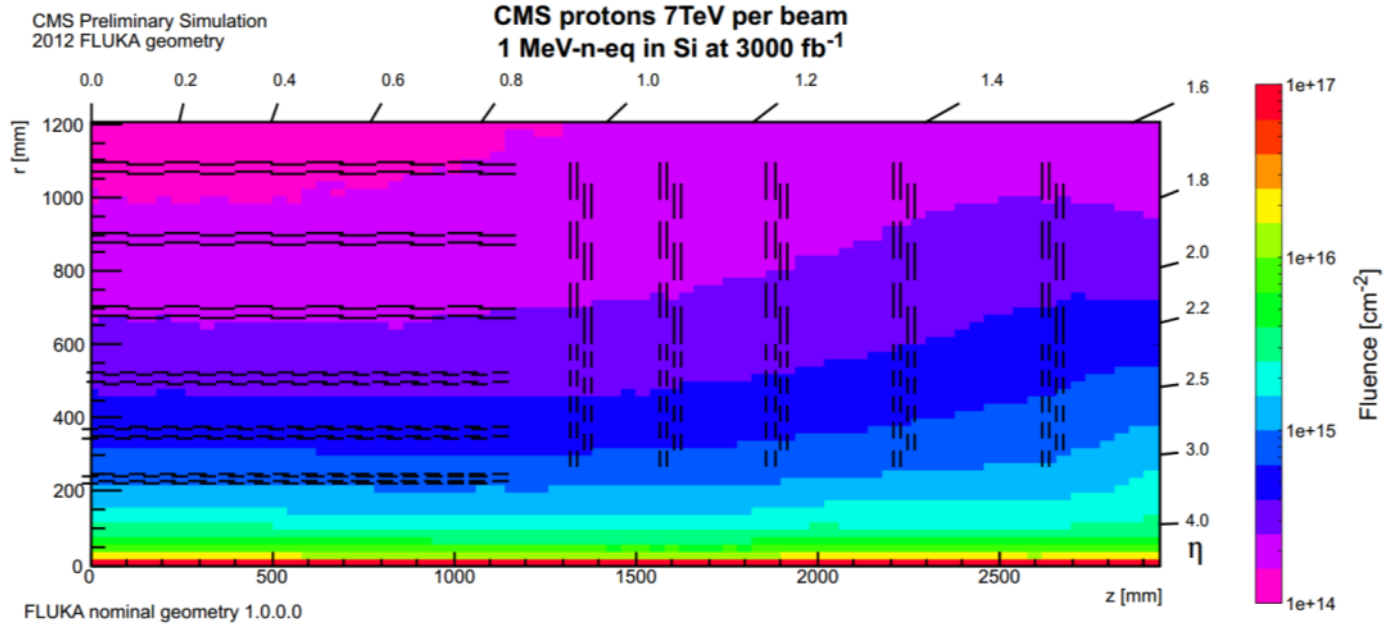
HL-LHC dose



< 3e+05 Gy = 30 Mrad

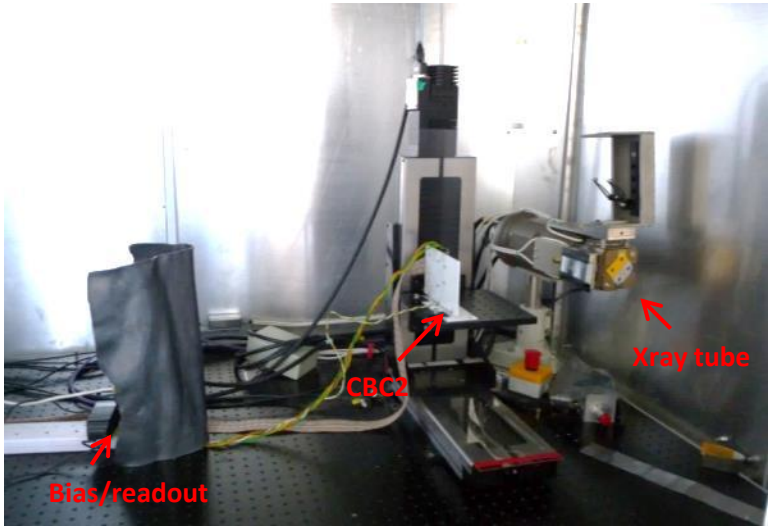
NB: calculated for 3000 fb^{-1} but with present Tracker

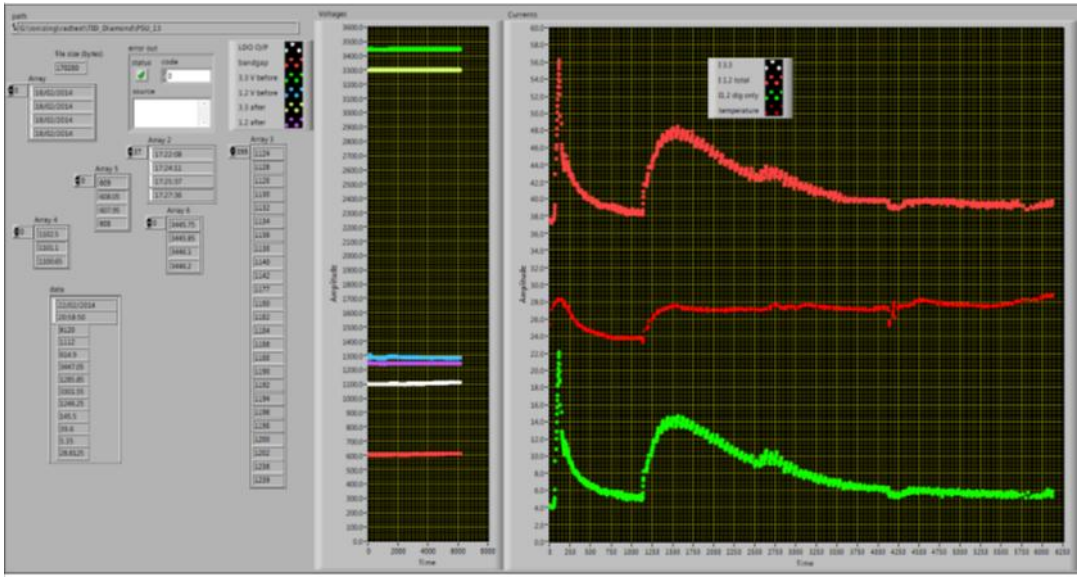
https://twiki.cern.ch/twiki/bin/view/CMSPublic/BRILRadiationSimulation

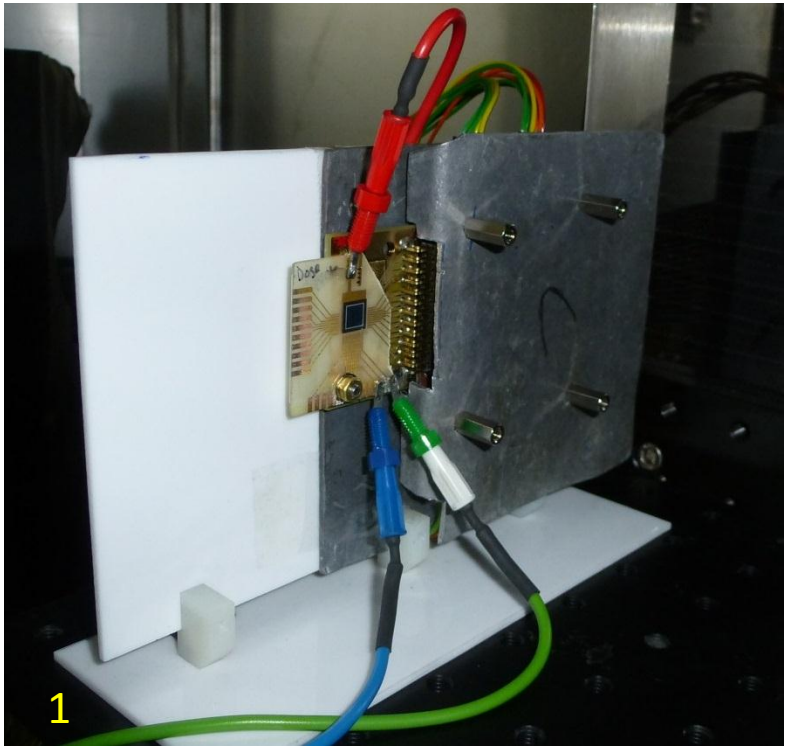


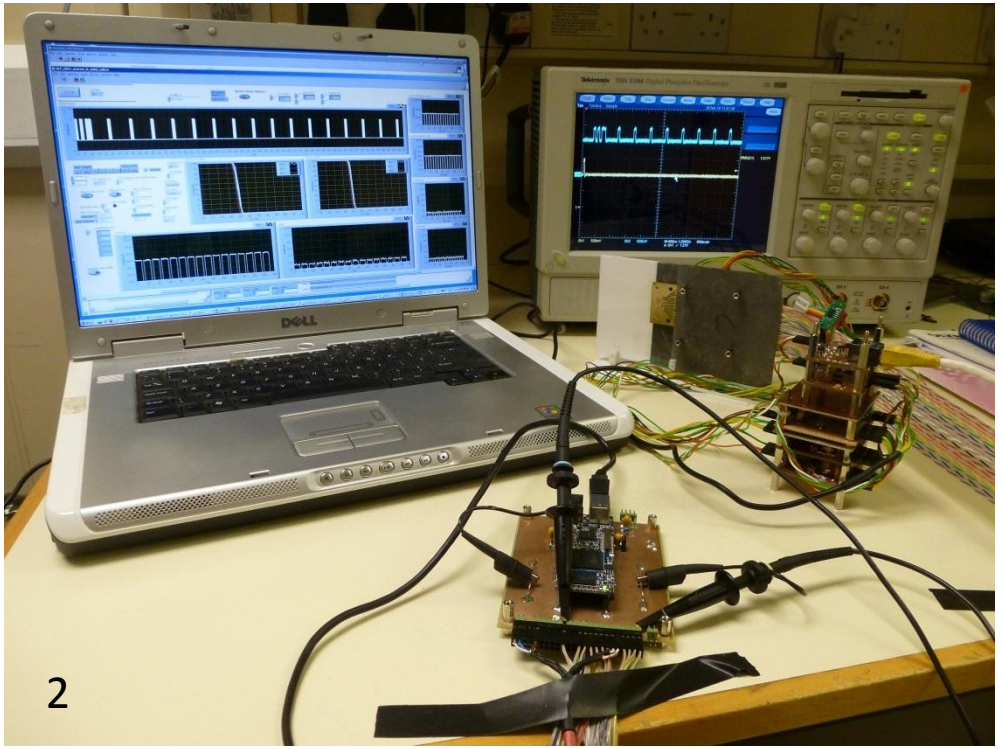
Total Ionizing Dose test

- First xray irradiation to 10 Mrads
- CBC2 operated continuously during irradiation
- monitored currents, biases, pedestal, noise
- no significant change in performance, moderate increase in current before annealing
- Next: TID test up to ~50 Mrads






1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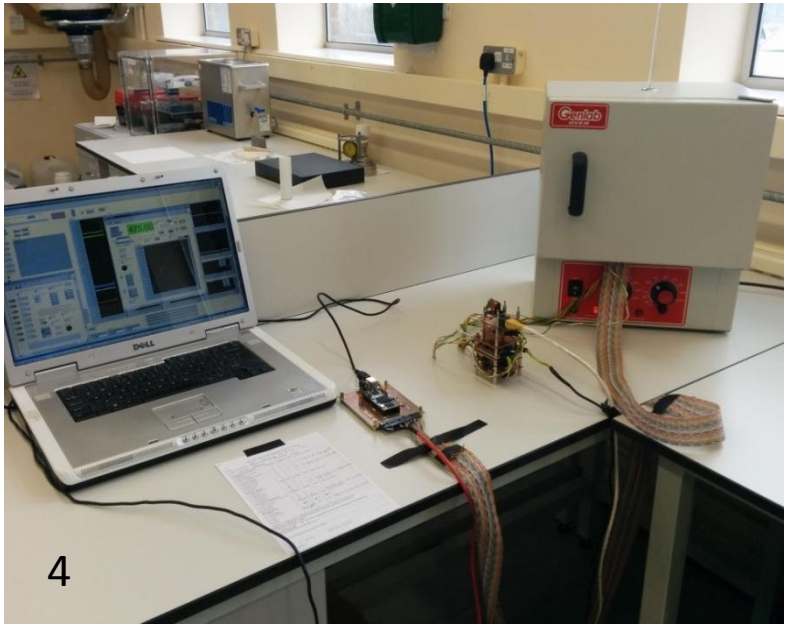
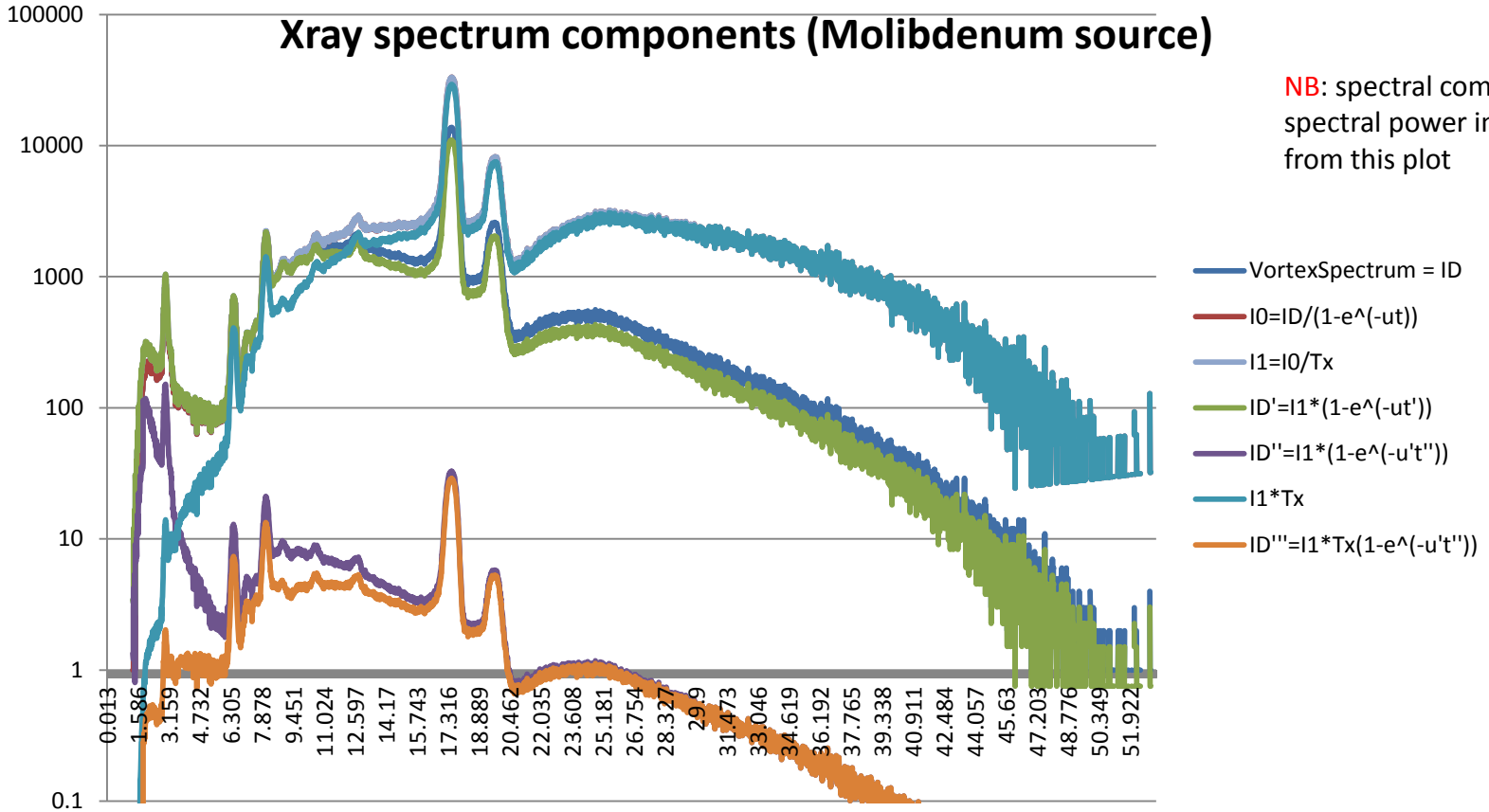
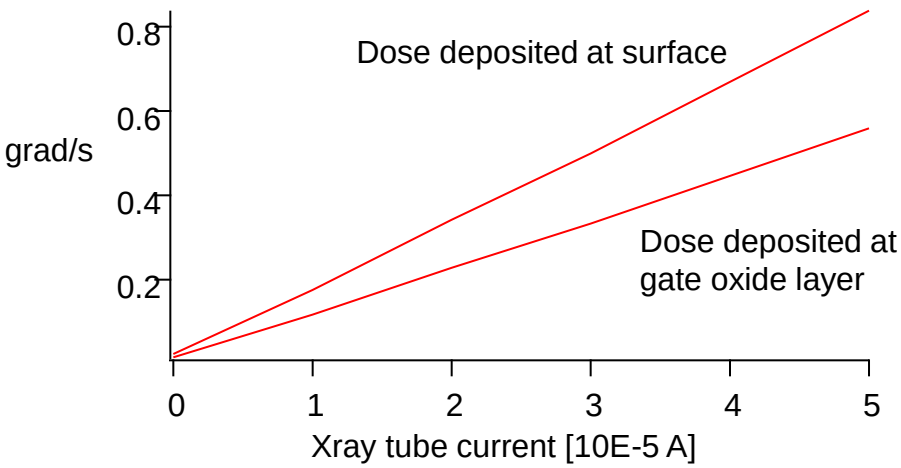
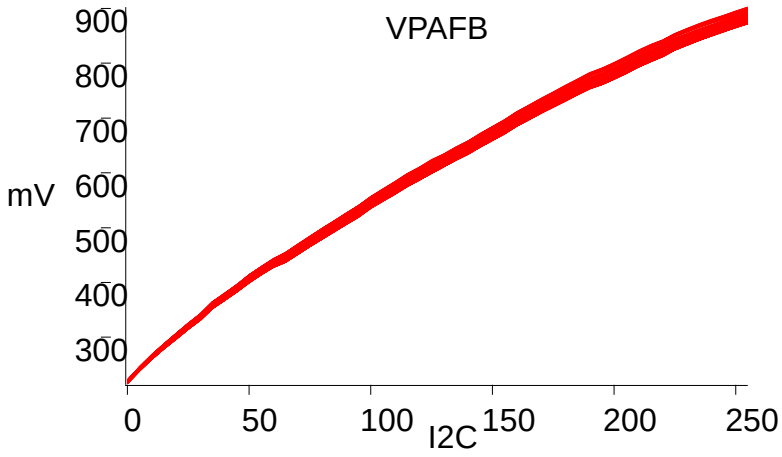

4


Vortex
CAUTION CONTAINS BERYLLIUM WINDOW
OUT
DLS
DDG00000047
3



NB: spectral component accurate, spectral power information missing from this plot





Conclusions and Future Work

CBC3: the final prototype

Sensor choice:

n-on-p, AC coupled, strip length up to 8 cm (~12 pF)

=> polarity defined, no DC sink/source requirement

Front end amplifier:

- adjust for 1V VDDA
- re-examine pulse shape for dead-time issue
  want pulse that returns to baseline within 50 ns
  some overshoot unavoidable
- adjust preamplifier for larger sensor capacitance

To maintain current noise performance for 8cm strips:

$$\text{noise} \propto \frac{C}{\sqrt{I_{DS}}} \text{ , } g_m \propto I_{DS}$$

→ to compensate (8/5) x C need 2.6x current in input device!

Comparator:

- Possibility to include 2 comparators/channel:
  5σ and 3σ thresholds
- (1 chan > 5σ) OR (2 neighbours > 3σ)=> hit
  → more signals to cross chip boundaries
  →extra ~50uW/channel
- Additional circuit to suppress HIPs (block comp. out if longer than several BXs)

Trigger Rate & Latency:

- Pipeline length increase to 12 - 25µsec
- L1 Trigger rate increase: 500kHz - 1MHz

Channel masking:

Sparsification (in concentrator) becomes mandatory for 1 MHz trigger rate

Stub definition:

- ½ strip cluster resolution → 8b address
- 5b bend information
- priority selection of 3 highest-pT stubs
- Offset correction: 4 domains/chip (2 in CBC2)

Stub readout:

- 13b/stub, up to 3 stubs/BX
- 6 SLVS differential pairs @ 320Mbps

Changes to pad layout:

Considering relaxing the requirements for hybrid manufacturers by increasing the pitch of bump-bond pads

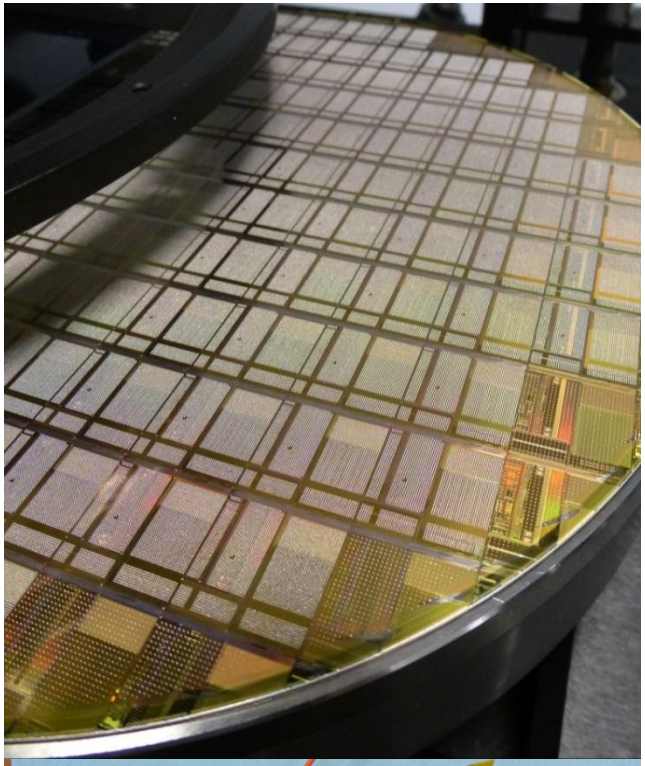
Summary & Conclusions

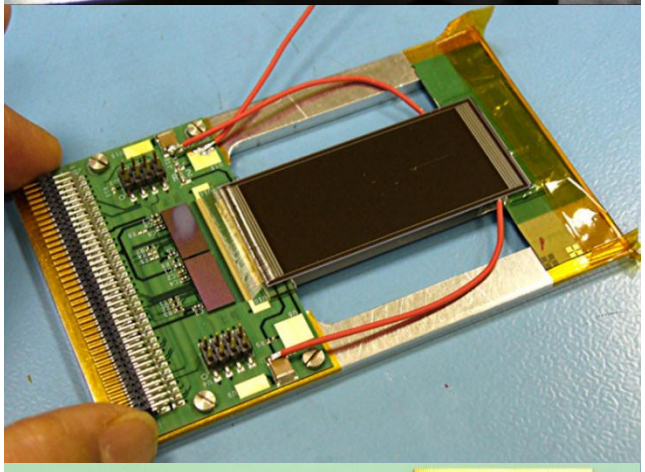
Two successful full-size prototypes of new Outer Tracker ASIC

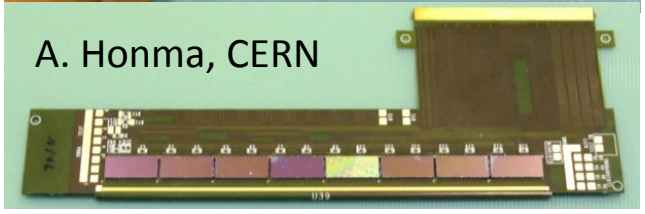
- ✓ CBC2 working to specs
- ✓ Some front-end improvements over CBC1
- ✓ Stub finding logic functioning
- ✓ Power features (LDO & DC-DC) operational

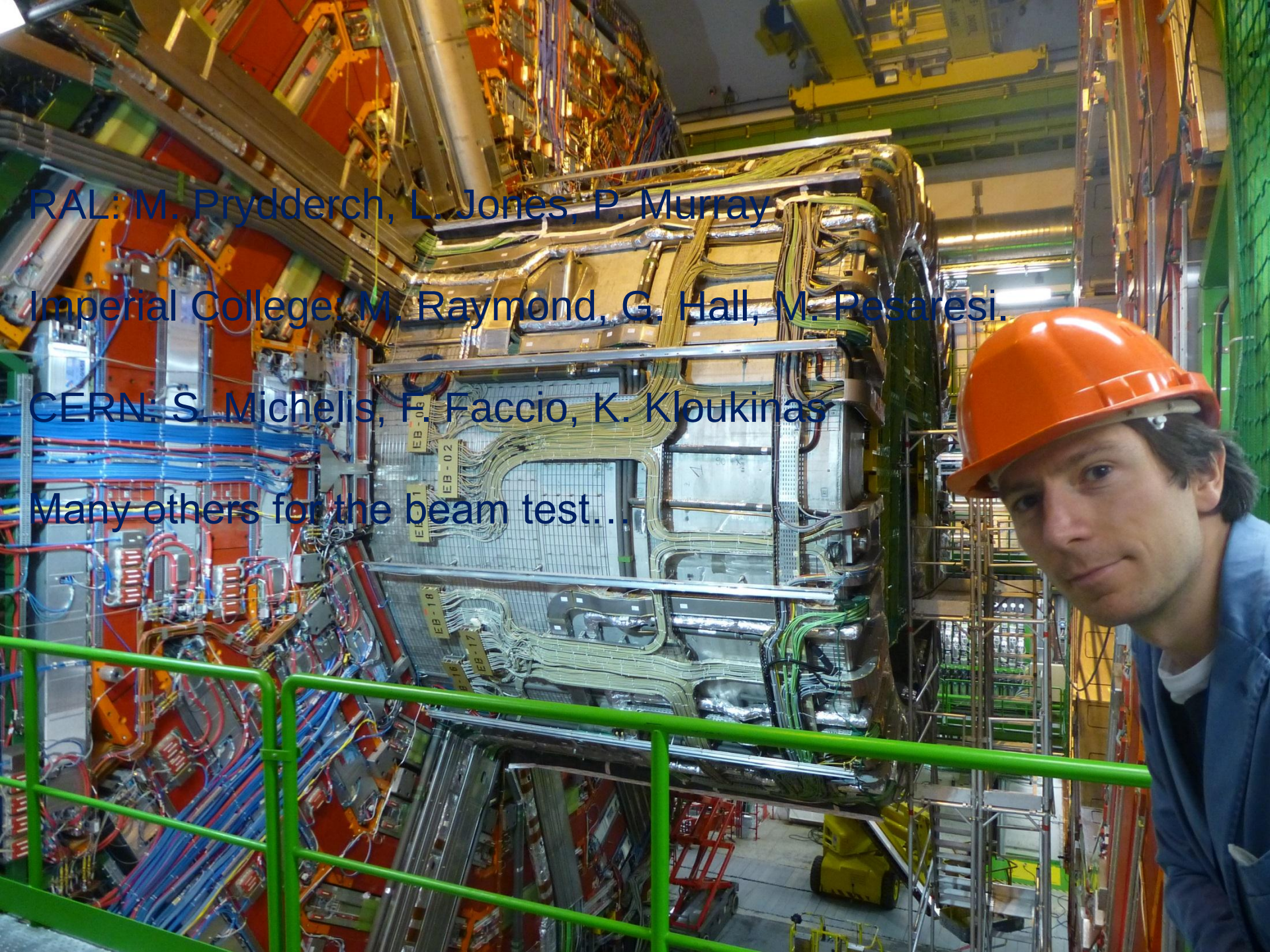
First prototype version of 2S module in hand

- ✓ First demonstration of bump-bonded ASIC for strip readout
- ✓ Ready to be distributed to collaborating institutes
- ✓ First beam test followed by ionizing radiation test and future SEU studies





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Many others for the beam test…